High Voltage Output, Low Noise Mono Class D Amplifier with AGC

■ General Description

OCA72390WPAD is a mono, filter-free Class D audio power amplifier with optimized automatic gain control (AGC) and 2X charge pump. AGC functions are not only configured to prevent audio signal distortion but also to enhance sound quality and volume automatically. It also can be configured to protect the speaker from damage at high power levels. The 2X charge pump architecture achieves high output voltage which can improve music signal dynamic range significantly. OCA72390WPAD is cable of driving 3.5W at 4.2V into a 6Ω load or 3.1W at 4.2V into an 8Ω load with speaker mode.

OCA72390WPAD also supports speaker and receiver 2-in-1 application. In receiver mode, the noise floor can be achieved 8.3μVrms and total harmonic distortion (THD) can be achieved 0.01% with 0.1W at 4.2V into an 8Ω load.

In addition to these features, I2C interface makes easier commutation between AP and OCA72390WPAD.

The device is a RoHs compliant WLCSP 2.43mm x 2.03mm -16B package.

■ Features

- Power Voltage Range: 2.7V to 5.5V
- Adaptive 2X Charge Pump architecture
- Support Speaker&Receiver 2-in-1 mode
- Overall Efficiency up to 81%
- Output power 3.1W@8Ω, 3.5W@6Ω,
- Low Noise:
  8.5μVrms (Class AB Receiver@0dB)
  14μVrms (Class D Speaker@4.5dB)
- PSRR: 90dB @ 217Hz
- Optimized AGC control for sound quality
- Excellent TDD noise suppression and POP-Click noise suppression
- Shut Down Current: 2 μA
- Support 1.2V I2C interface
- WLCSP-16B, 2.43mm x 2.03mm x 0.55mm

■ Applications

- Smartphones, Cellphone, PDAs
- Bluetooth, wireless handsets

■ Pin Configuration

WLCSP-16B (Top View)

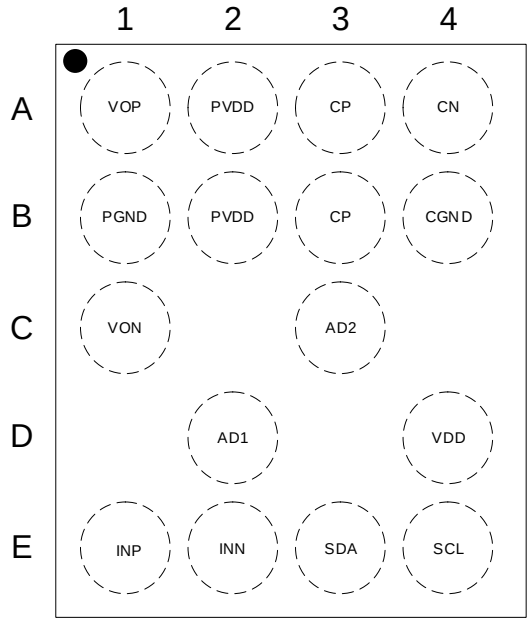


Figure 1, Pin Assignments of OCA72390WPAD

■ Pin Description

Pin No.	Pin Name	Pin Function
A1	VOP	Positive audio output
A2	PVDD	Charge pump output
A3	CP	Charge pump flying capacitance pin
A4	CN	Charge pump flying capacitance pin
B1	PGND	Power ground
B2	PVDD	Charge pump output
B3	CP	Charge pump flying capacitance pin
B4	CGND	Charge Pump power ground
C1	VON	Negative audio output
C3	AD2	I2C slave address pin2
D2	AD1	I2C slave address pin1
D4	VDD	Power supply
E1	INP	Positive audio input
E2	INN	Negative audio input
E3	SDA	I2C data
E4	SCL	I2C clock

■ Typical Application Circuit

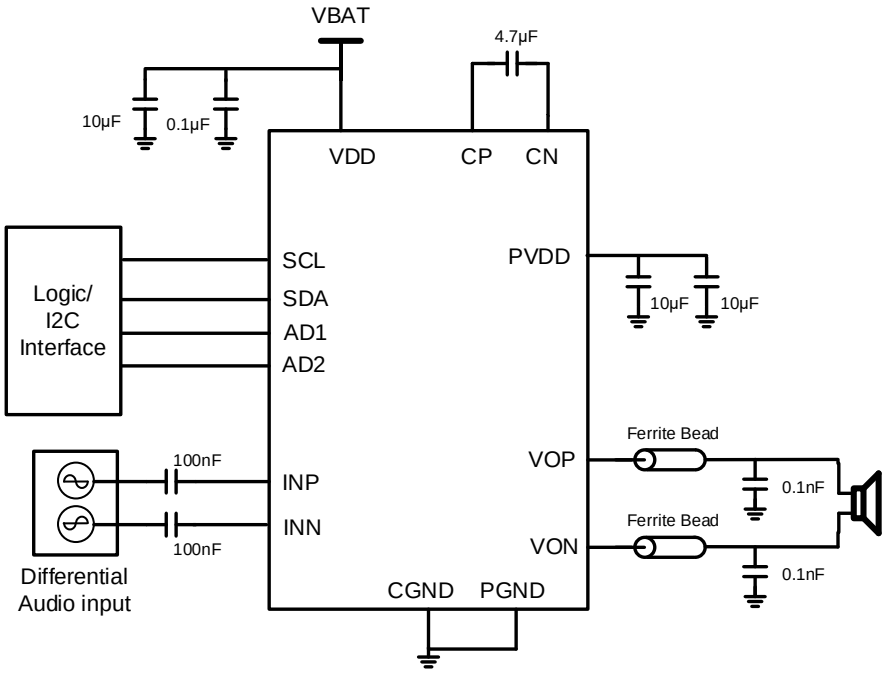


Figure 2, Typical Application Block diagram of OCA72390WPAD

■ Ordering Information

Part Number	Package Type	Mark	Package Qty	Temperature	Eco Plan	Ball
OCA72390WPAD	WLCSP-16B	LHA	3000pcs	-40~85°C	Green &RoHs	Sn/Ag/Cu

■ Block Diagram

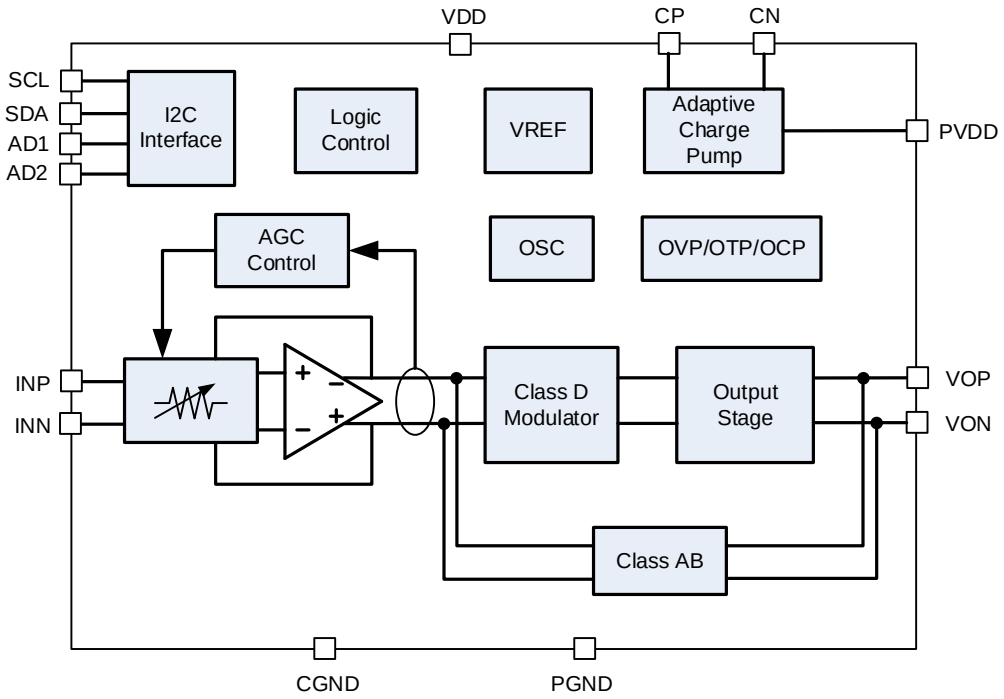


Figure 3, OCA72390WPAD Block Diagram

■ Absolute Maximum Ratings[1] (T_A=25°C unless otherwise noted)

Parameter	Symbol	Rating	Unit
Power Voltage Range	VDD	-0.3 to 6	V
Charge Pump Output Voltage Range	PVDD	-0.3 to 9.5	V
Input Voltage Range	INP, INN	-0.3 to VDD+0.3	V
Output Voltage Range	VOP, VON	-0.3 to PVDD+0.3	V
Charge Pump Flying Capacitance positive terminal Voltage Range	CP	-0.3 to PVDD+0.3	V
Charge Pump Flying Capacitance negative terminal Voltage Range	CN	-0.3 to VDD+0.3	V
Minimum load Resistance	R_L	5	Ω
Human Body Model	HBM	±4	kV
Charged Device Model	CDM	±1.5	kV
Storage Temperature Range	T_S	-65 to +150	°C
Maximum Operating Junction Temperature Range	T_J	-40 to 125	°C

Note1: Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

■ Recommended Operating Conditions[2](T_A=25°C unless otherwise noted)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	VDD	2.7 ~ 5.5	V
Ambient Operating Temperature	T_A	-40 to 85	°C
Thermal Resistance	$R_{\theta JA}$	60	°C/W

Note2: The device is not guaranteed to function outside of its operating conditions

■ Electrical Characteristics

(Unless otherwise noted, typical values are at T_A=25°C, VDD= 3.6V, R_L= 8Ω+33μH, f=1kHz)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VDD	Power Supply Voltage		2.7		5.5	V
V_{UVLO}	Under-Voltage Lockout Threshold			2.5		V
$V_{UVLO-HYS}$	UVLO hysteresis voltage			100		mV
I_{SD}	Shutdown current	VDD=3.6V		2	5	μA
T_{ON}	Turn-on Time			45		ms
ADP Charge Pump						
PVDD	Charge Pump Output Voltage[3]	VDD=2.7V to 4V, OVP=8V		2*VDD		V
		VDD> 4V, OVP=8V		8		V
	Charge Pump Output Voltage at Adaptive mode	P_O<P_{TH}		VDD		V
		P_O≥P_{TH}, VDD=2.7V to 4V, OVP=8V		2*VDD		V
V_{OVP}	Over Voltage Protection Threshold[3]	VDD ≥ 4V		8		V
$V_{OVP-HYS}$	OVP hysteresis voltage	VDD ≥ 4V		50		mV
F_{CP}	Charge Pump Operation Frequency	VDD=2.7V to 4V		1.6		MHz
T_{ST}	Soft Start Time	C_{OUT}=4.7μF, No Loading		0.5		ms
η	Charge Pump Efficiency	VDD=4.2V, I_{LOAD}=200mA		90		%
Speaker Mode with Class D path						
V_{OS}	Output offset voltage	AC ground input	-30		30	mV
η_T	Speaker Mode Total Efficiency	VDD=4.2V, P_O=2.5W, R_L=8Ω+33μH		81		%
I_Q	Speaker Quiescent Current	VDD=3.6V, Input ac ground. R_L=8Ω+33μH, OVP=8V		12.1		mA
V_{IN}	Recommend Input Signal Amplitude	VDD=2.7V to 5.5V			1	Vp
F_{OSC}	Modulation Frequency	VDD=2.7V to 5.5V		800		kHz
P_{AGC}	AGC Power[3]	R_L=8Ω+33μH	0.72	0.8	0.88	W
		R_L=6Ω+33μH	0.96	1.067	1.17	
PSRR	Power Supply Rejection Rate	VDD=4.2V, Vpp-sin=200mV, f=217Hz		-80		dB
		VDD=4.2V, Vpp-sin=200mV, f=1kHz		-75		
A_V	Speaker Gain[3]	VDD=2.7V to 5.5V		24		dB
SNR	Signal-to-Noise Ratio	VDD=4.2V, P_O=3.2W, R_L=8Ω+33μH, A_V=18dB, THD+N=1%, OVP=8V		102		dB
		VDD=4.2V, P_O=0.8W, R_L=8Ω+33μH, A_V=18dB, THD+N=1%, OVP=8V		94		
E_N	Speaker Output Noise	20Hz to 20kHz, input AC ground with A-weighting filter, A_V=24dB		47		μVrms
		20Hz to 20kHz, input AC ground with A-weighting filter, A_V=18dB		35		μVrms

R_{IN}	Speaker Input Inner Resistance	A_V=24dB		9.9		kΩ
		A_V=18dB		19		
F_{IN}	Speaker Input Cut-off Frequency	C_{IN}=47nF, A_V=24dB		342		Hz
		C_{IN}=47nF, A_V=18dB		178		
		C_{IN}=68nF, A_V=24dB		236		
		C_{IN}=68nF, A_V=18dB		124		
		C_{IN}=100nF, A_V=24dB		160		
		C_{IN}=100nF, A_V=18dB		84		
THD+N	Total Harmonic Distortion + Noise	VDD=4.2V, P_O=0.6W, OVP=8V R_L=8Ω+33μH, f=1kHz		0.01		%
P_O	Speaker Output Power	THD+N=1%, R_L=8Ω+33μH, VDD=4.2V, OVP=8V		3.1		W
		THD+N=10%, R_L=8Ω+33μH, VDD=4.2V, OVP=8V		3.6		
		THD+N=1%, R_L=6Ω+33μH, VDD=4.2V, OVP=8V		3.5		
		THD+N=10%, R_L=6Ω+33μH, VDD=4.2V, OVP=8V		4.2		
Speaker Mode with Class AB path						
V_{OS}	Output offset voltage	AC ground input	-30		30	mV
η_T	Speaker Mode Total Efficiency	VDD=4.2V, P_O=1.2W, R_L=8Ω+33μH, OVP=6V			40	%
		VDD=4.2V, P_O=0.8W, R_L=8Ω+33μH			68	%
I_Q	Speaker Quiescent Current	VDD=3.6V, Input AC Ground, R_L=8Ω+33μH, OVP=6V		11		mA
		VDD=3.6V, Input AC Ground, R_L=8Ω+33μH,		4.7		mA
V_{IN}	Recommend Input Signal Amplitude	VDD=2.7V to 5.5V			1	Vp
P_{AGC}	AGC Power[3]	R_L=8Ω+33μH	0.72	0.8	0.88	W
		R_L=6Ω+33μH	0.96	1.067	1.17	W
PSRR	Power Supply Rejection Rate	VDD=4.2V, Vpp-sin=200mV, 217Hz		80		dB
		VDD=4.2V, Vpp-sin=200mV, 1kHz		82		dB
A_V	Speaker Gain[3]	VDD=2.7V to 5.5V		24		dB
SNR	Signal-to-Noise Ratio	VDD=3.6V, P_O=1.2W, R_L=8Ω+33μH, OVP=6V, 18dB		97		dB
		VDD=3.6V, P_O=0.8W, R_L=8Ω+33μH, OVP=6V, 18dB		95		dB
E_N	Speaker Output Noise	20Hz to 20kHz, input AC ground with A-weighting filter, A_V=24dB		45		μVrms
		20Hz to 20kHz, input AC ground with A-weighting filter, A_V=18dB		34		μVrms
R_{IN}	Speaker Input Inner Resistance	A_V=24dB		9.9		kΩ
		A_V=18dB		19		kΩ

F_{IN}	Speaker Input Cut-off Frequency	C_{IN}=47nF, A_V=24dB		342		Hz
		C_{IN}=47nF, A_V=18dB		178		
		C_{IN}=68nF, A_V=24dB		236		
		C_{IN}=68nF, A_V=18dB		124		
		C_{IN}=100nF, A_V=24dB		160		
		C_{IN}=100nF, A_V=18dB		84		
THD+N	Total Harmonic Distortion + Noise	VDD=4.2V, P_O=1.2W, OVP=6V R_L=8Ω+33μH, f=1kHz		0.3		%
P_O	Speaker Output Power	THD+N=1%, R_L=8Ω+33μH, VDD=4.2V, OVP=6V		2.1		W
		THD+N=10%, R_L=8Ω+33μH, VDD=4.2V, OVP=6V		2.6		
		THD+N=1%, R_L=8Ω+33μH, VDD=4.2V		0.94		
		THD+N=10%, R_L=8Ω+33μH, VDD=4.2V		1.18		
Receiver Mode						
I_Q	Receiver Mode Quiescent Current with Class D path	VDD=3.6V, Input ac ground. R_L=8Ω+33μH		5.5		mA
	Receiver Mode Quiescent Current with Class AB path	VDD=3.6V, Input ac ground. R_L=8Ω+33μH		3.5		mA
η_T	Receiver Mode Total Efficiency with Class D path	VDD=4.2V, P_O=0.8W, R_L=8Ω+33μH		88		%
	Receiver Mode Total Efficiency with Class AB path	VDD=4.2V, P_O=0.8W, R_L=8Ω+33μH		47		%
A_V	Receiver Mode Gain with Class D path[3]	VDD=2.7V to 5.5V		4.5		dB
	Receiver Mode Gain with Class AB path[3]	VDD=2.7V to 5.5V		0		dB
R_{IN}	Input Inner Resistance with Class D path	A_V=4.5dB		48		kΩ
	Input Inner Resistance with Class AB path	A_V=0dB		72		
F_{IN}	Receiver Mode Input Cut-off Frequency with Class D	C_{IN}=47nF, A_V=4.5dB		70		Hz
		C_{IN}=68nF, A_V=4.5dB		49		
		C_{IN}=100nF, A_V=4.5dB		33		
	Receiver Mode Input Cut-off Frequency with Class AB	C_{IN}=47nF, A_V=0dB		47		
		C_{IN}=68nF, A_V=0dB		33		
		C_{IN}=100nF, A_V=0dB		22		

E_N	Receiver Mode Output Noise with Class D path	20Hz to 20kHz, input AC ground with A-weighting filter, A_V=4.5dB		14		μVrms
	Receiver Mode Output Noise with Class AB path	20Hz to 20kHz, input AC ground with A-weighting filter, AV=0dB		8.5		
THD+N	Total Harmonic Distortion + Noise with Class D path	VDD=4.2V, P_O=0.1W, R_L=8Ω+33μH, f=1kHz		0.01		%
	Total Harmonic Distortion + Noise with Class AB path	VDD=4.2V, P_O=0.1W, R_L=8Ω+33μH, f=1kHz		0.15		%
PSRR	Power Supply Rejection Rate with Class D path	VDD=4.2V, Vpp-sin=200mV, 217Hz		78		dB
		VDD=4.2V, Vpp-sin=200mV, 1kHz		67		
	Power Supply Rejection Rate with Class AB path	VDD=4.2V, Vpp-sin=200mV, 217Hz		93		
		VDD=4.2V, Vpp-sin=200mV, 1kHz		88		
P_O	Receiver Mode Output Power with Class D path	THD+N=1%, R_L=8Ω+33μH, VDD=4.2V,		0.98		W
		THD+N=10%, R_L=8Ω+33μH, VDD=4.2V,		1.21		
	Receiver Mode Output Power with Class AB path	THD+N=1%, R_L=8Ω+33μH, VDD=4.2V,		0.48		
		THD+N=10%, R_L=8Ω+33μH, VDD=4.2V,		0.67		
ADP Mode						
I_Q	Speaker Quiescent Current at ADP CP MODE	VDD=3.6V, Input ac ground. R_L=8Ω+33μH, OVP=8V		7.0		mA
P_{TH}	Output Power Threshold[3]	VDD=2.7~5.5V,R_L=8Ω+33μH, OVP=8V		0.3		W
η_T	Speaker Mode Total Efficiency (CP + Class D)	VDD=3.6V, P_O=2.5W, R_L=8Ω+33μH, OVP=8V		80		%
		VDD=3.6V, P_O=0.3W, R_L=8Ω+33μH, OVP=8V		77		%
PSRR	Power Supply Rejection Rate	VDD=4.2V, Vpp-sin=200mV, 217Hz		77		dB
		VDD=4.2V, Vpp-sin=200Mv, 1kHz		76		dB
E_N	Speaker Output Noise	20Hz to 20kHz, input AC ground with A-weighting filter, A_V=24dB		45		μVrms
		20Hz to 20kHz, input AC ground with A-weighting filter, A_V=18dB		35		μVrms
THD+N	Total Harmonic Distortion + Noise	VDD=4.2V,P_O=0.6W,OVP=6V R_L=8Ω+33μH, f=1kHz		0.02		%
Automatic Gain Control (AGC)						
T_{AT_Lim}	Limiter Attack Time[3]			0.08		ms/dB
T_{AT_Fast}	Fast AGC Attack Time[3]			0.64		ms/dB
T_{AT_Slow}	Slow AGC Attack Time[3]			41		ms/dB
T_{RLT}	Slow AGC Release Time[3]			21		ms/dB
A_{MAX}	The Maximum Attenuation Gain	VDD=2.7V to 5.5V		-13.5		dB
Thermal Information						

T_{SHDN}	Thermal Shutdown Temperature			160		°C
T_{REC}	Thermal Protection Recovery Temperature			130		°C
I/O Interface						
V_{IH}	High Level Input Voltage of SCL, SDA, AD1, AD2		1		VDD	V
V_{IL}	Low Level Input Voltage of SCL, SDA, AD1, AD2				0.4	V

Note3: Registers are adjustable; Refer to the list of registers.

I²C Compatible Timing Specifications[4] (SCL, SDA), see Figure 4						
f_{SCL}	SCL clock frequency	Standard Mode	-	-	100	KHz
		Fast Mode	-	-	400	KHz
t_{LOW}	Low period of the SCL clock	Standard Mode	4.7	-	-	μs
		Fast Mode	1.3	-	-	μs
t_{HIGH}	High period of the SCL clock	Standard Mode	4.0	-	-	μs
		Fast Mode	0.6	-	-	μs
t_{BUF}	Bus free time between a STOP and START condition	Standard Mode	4.7	-	-	μs
		Fast Mode	1.3	-	-	μs
$t_{HD,STA}$	Hold time for a repeated START condition	Standard Mode	4.0	-	-	μs
		Fast Mode	0.6	-	-	μs
$t_{SU,STA}$	Setup time for a repeated START condition	Standard Mode	4.7	-	-	μs
		Fast Mode	0.6	-	-	μs
$t_{SU,DAT}$	Data setup time	Standard Mode	0.25	-	-	μs
		Fast Mode	0.1	-	-	μs
$t_{HD,DAT}$	Data hold time	Standard Mode	0.05	-	3.45	μs
		Fast Mode	0.05	-	0.9	μs
t_{RCL1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	Standard Mode	-	-	1000	ns
		Fast Mode	-	-	1000	ns
t_{RCL}	Rise time of SCL signal	Standard Mode	-	-	1000	ns
		Fast Mode	-	-	300	ns
t_{FCL}	Fall time of SCL signal	Standard Mode	-	-	300	ns
		Fast Mode	-	-	300	ns
t_{RDA}	Rise time of SDA signal	Standard Mode	-	-	1000	ns
		Fast Mode	-	-	300	ns
t_{FDA}	Fall time of SDA signal	Standard Mode	-	-	300	ns
		Fast Mode	-	-	300	ns
$t_{SU,STO}$	Setup time for STOP condition	Standard Mode	4.0	-	-	μs
		Fast Mode	0.6	-	-	μs
C_B	Capacitive load for SCL and SDA		-	-	0.4	nF

Note4: OCA72390 is guaranteed to meet performance specifications over the –40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.

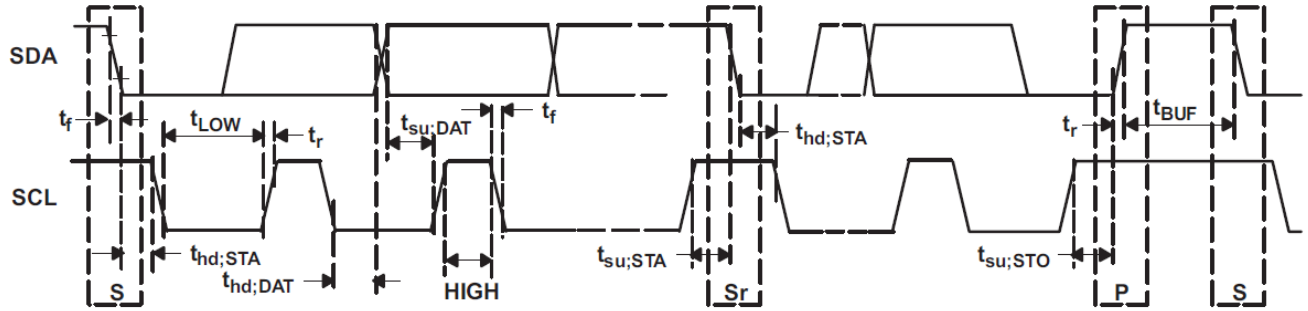
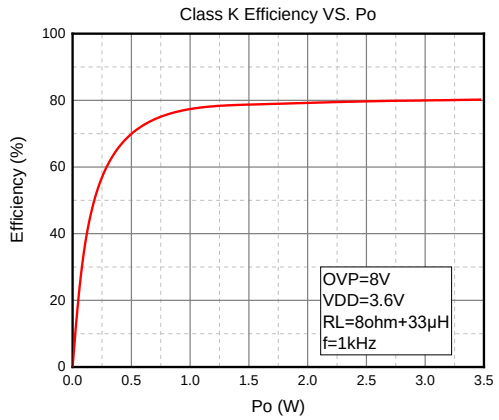
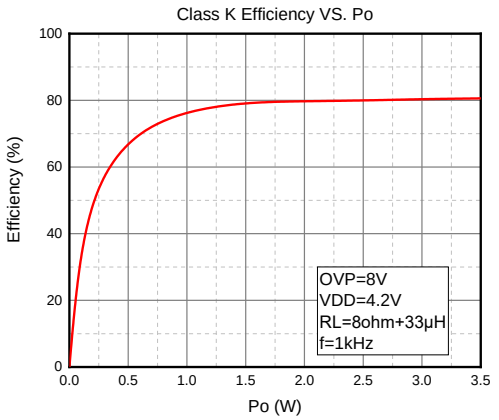
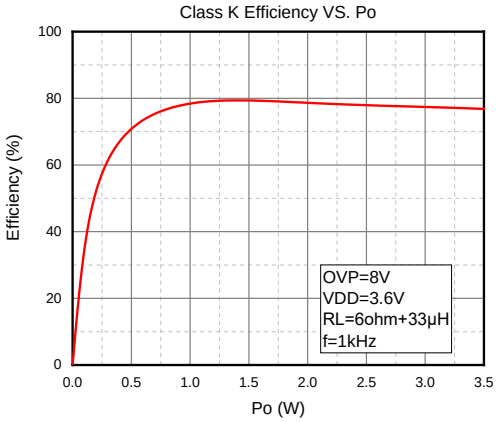


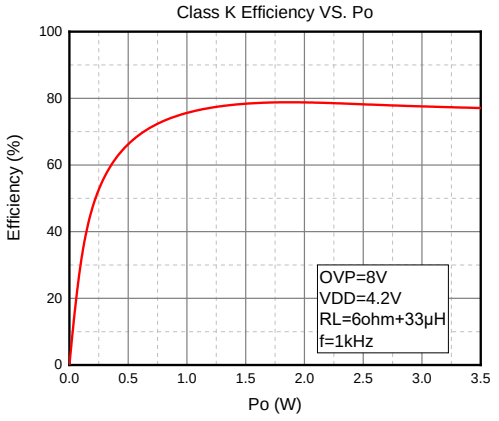
Figure 4, Serial Interface Timing for F/S-Mode I2C

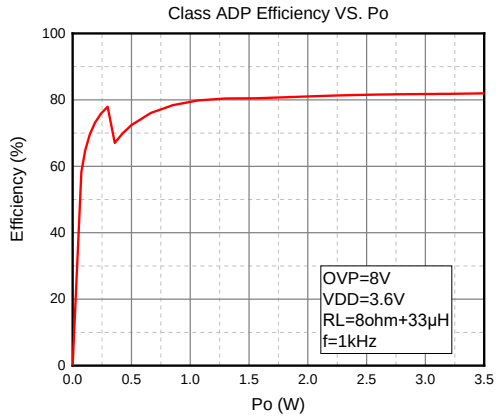
■ Typical characteristics

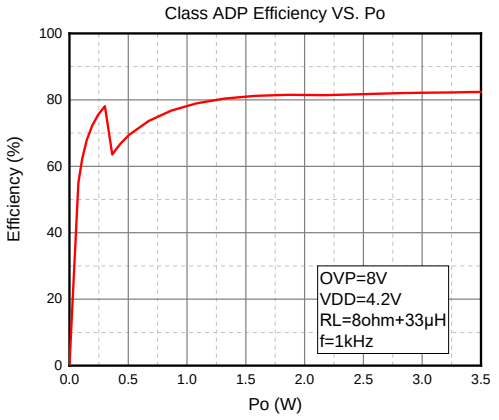




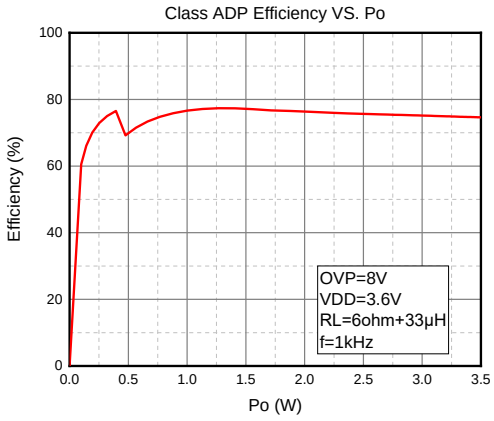


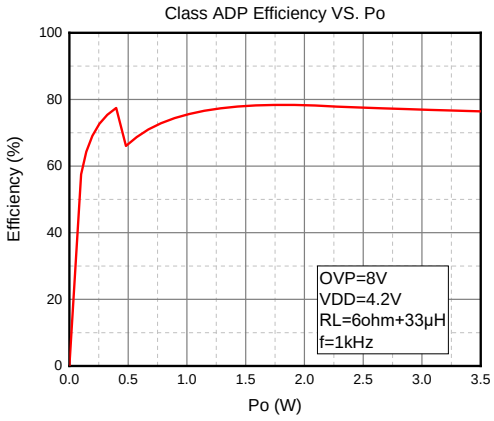


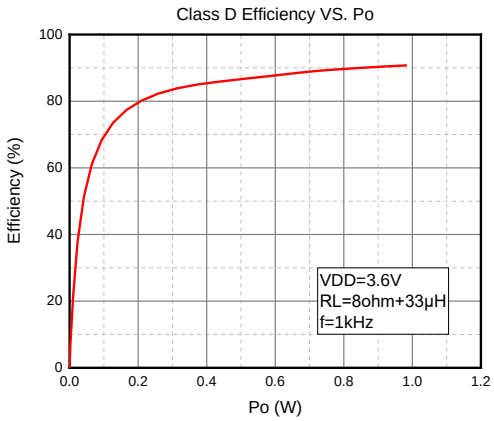


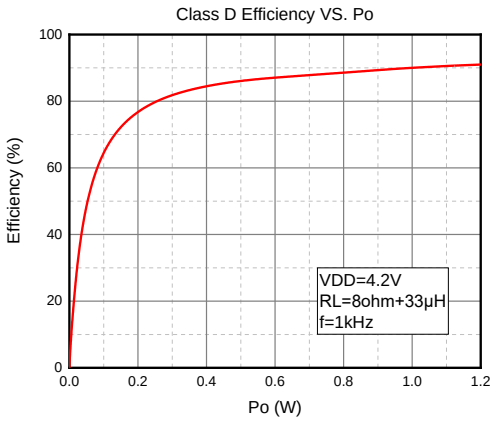


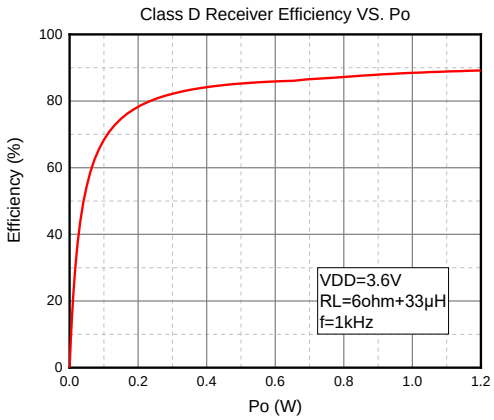
■ Typical characteristics (continued)

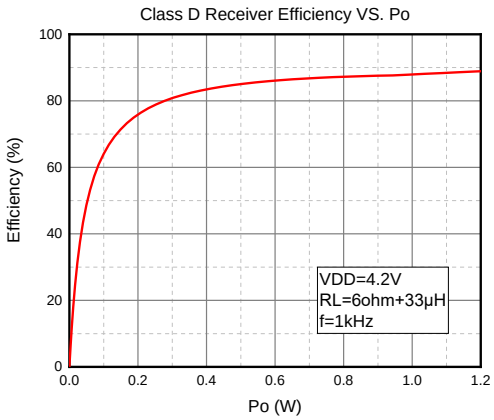




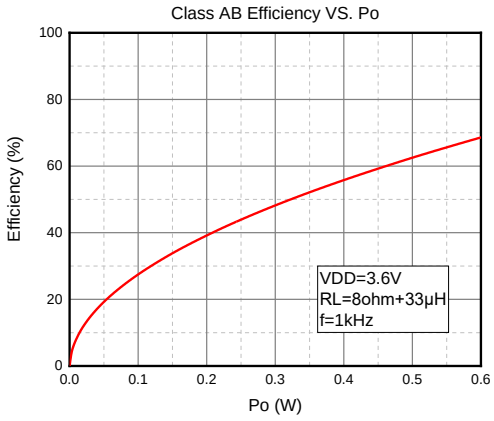


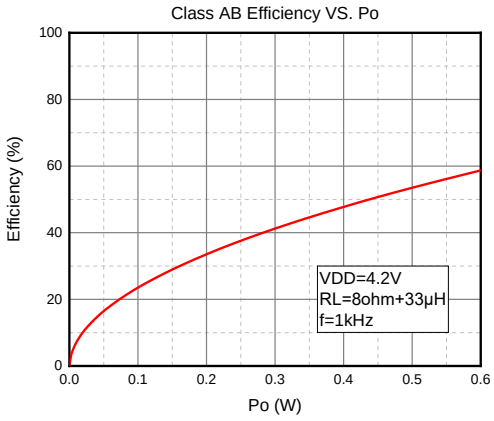


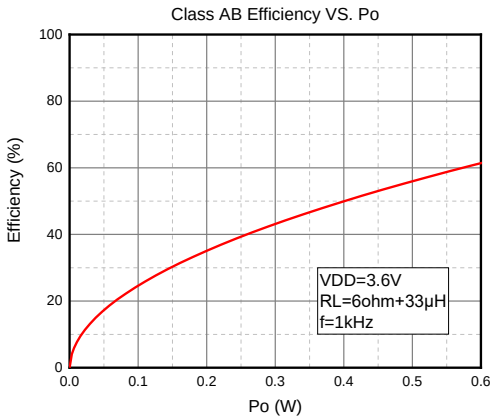


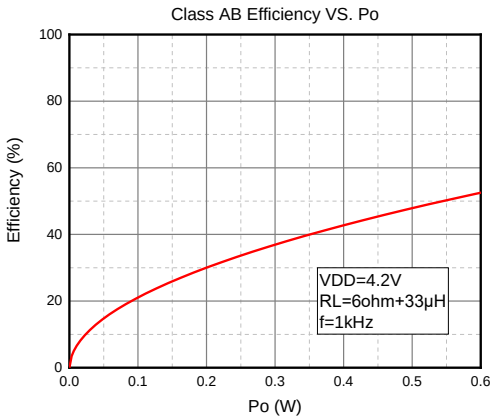


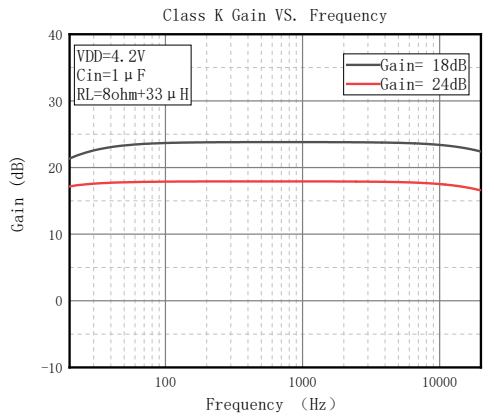
■ Typical characteristics（continued)

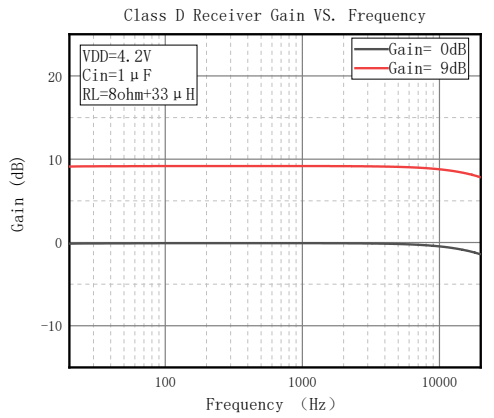












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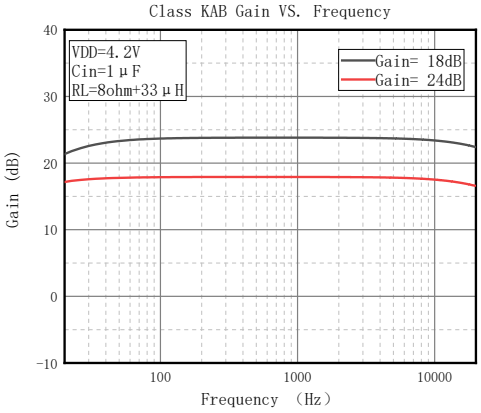
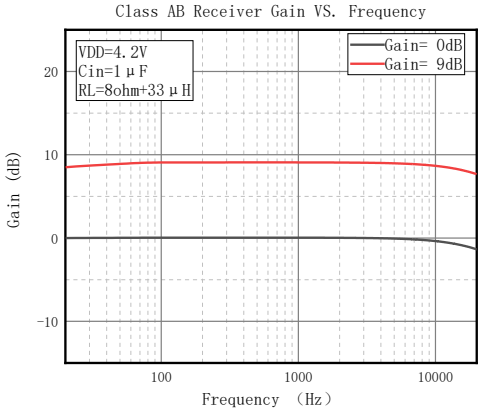
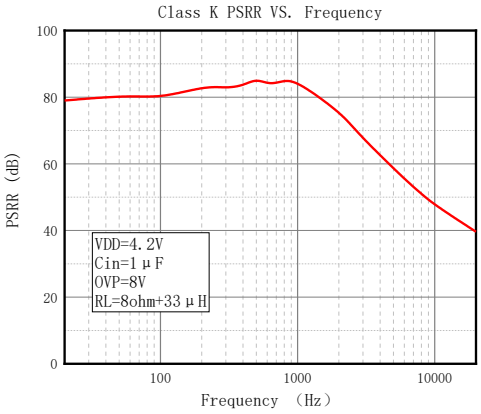
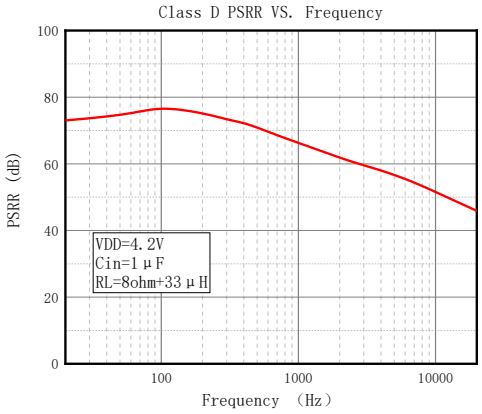
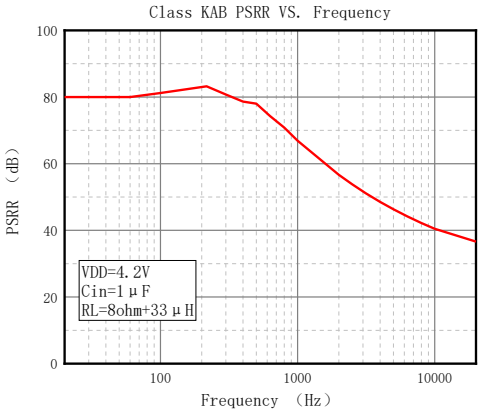
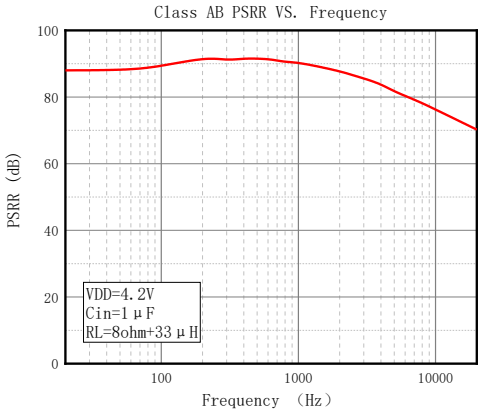




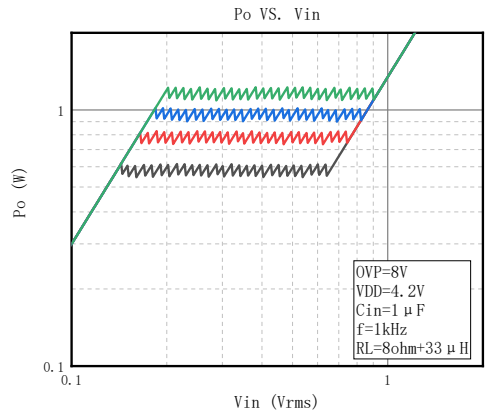


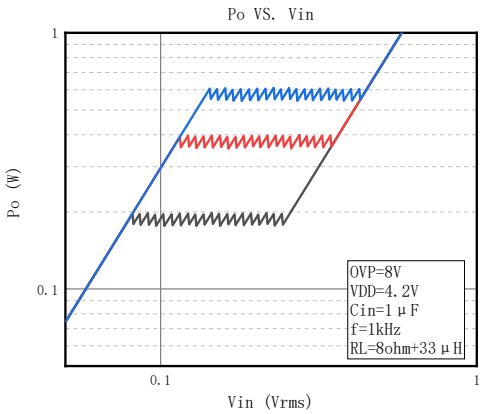


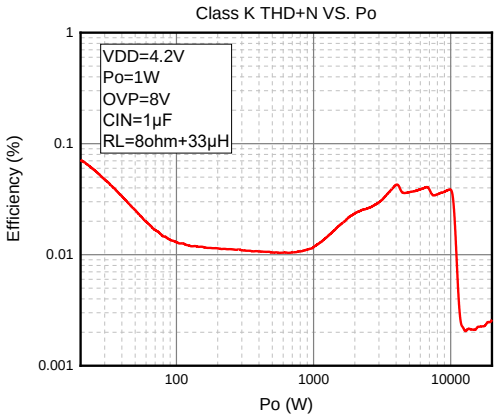


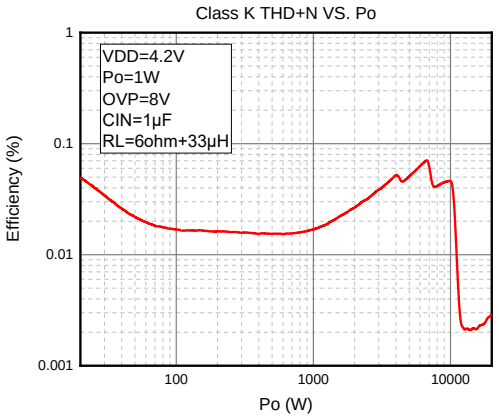


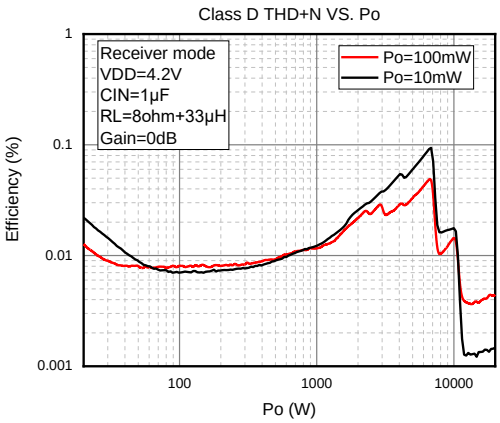
■ Typical characteristics（continued)

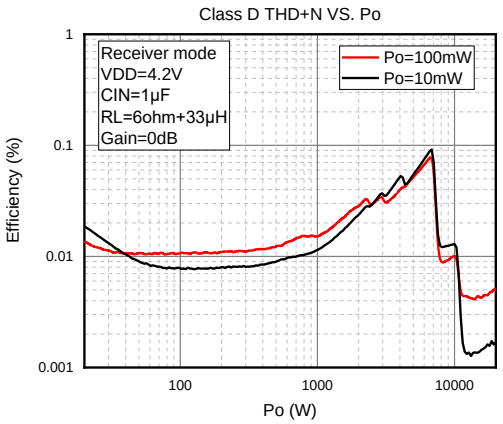




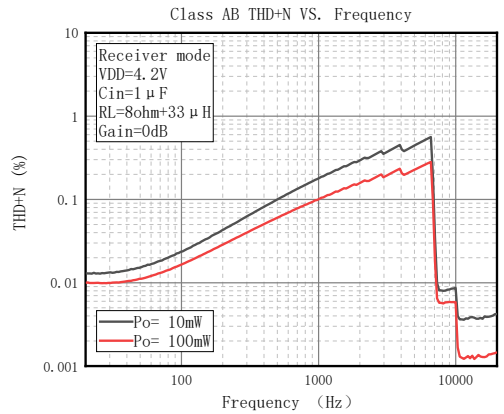


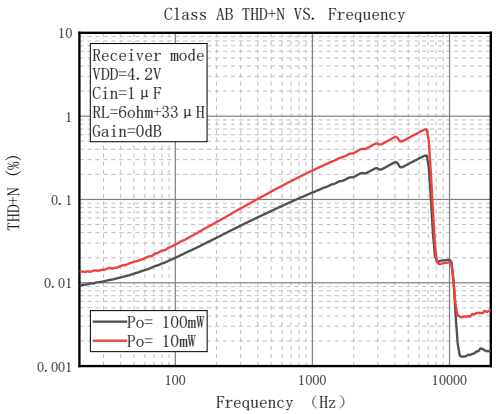




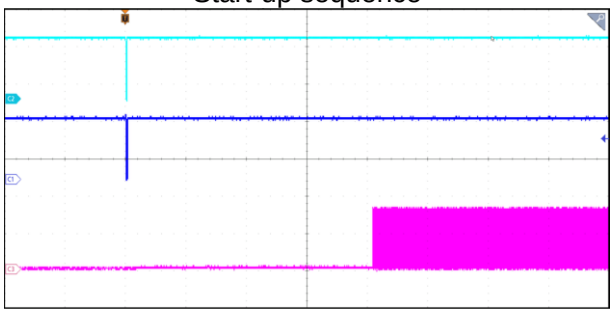


■ Typical characteristics（continued)



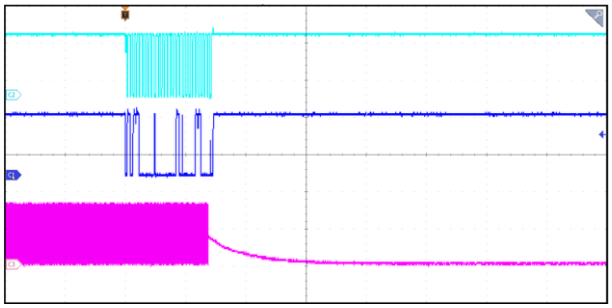


Start-up sequence



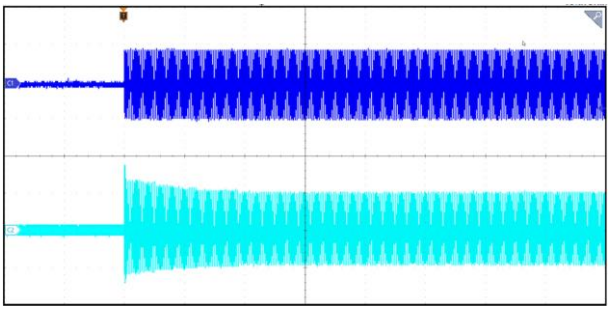
10ms / div

Shutdown sequence



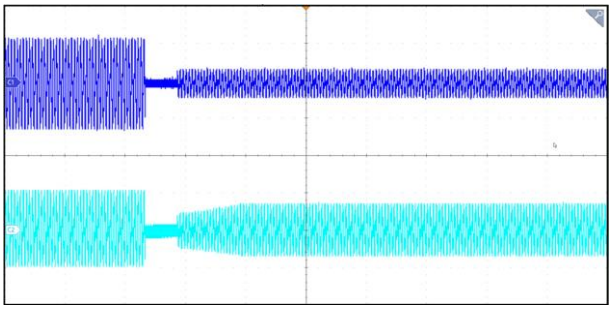
200μs / div

Triple-level Triple Rate AGC Attack Timing



200ms / div

Triple-level Triple Rate AGC Release Timing



100ms / div

■ Detail Description

OCA72390WPAD is a mono, filter-free Class D audio power amplifier with optimized automatic gain control (AGC) and charge pump. AGC functions are not only configured to prevent audio signal distortion but also to enhance sound quality and volume automatically. It also can be configured to protect the speaker from damage at high power levels. The high voltage boost achieves high output voltage which can improve music signal dynamic range significantly. OCA72390WPAD also supports speaker and receiver 2-in-1 application. In receiver mode, the noise floor can be achieved 11μVrms and total harmonic distortion (THD) can be achieved 0.01% with 0.1W at 4.2V into an 8Ω load. The AGC/Charge pump function is programmable via a digital I2C interface.

Automatic Gain Control

The Automatic Gain Control (AGC) feature provides continuous automatic gain adjustment to the amplifier through an internal programable gain control circuit. This feature enhances the perceived audio loudness and at the same time prevents speaker damage from occurring (Limiter function).

The AGC function is implemented by Limiter, Fast AGC and Slow AGC. It detects the audio input signal and change internal gain to modify output signal amplitude. The gain step of AGC is 0.5dB. The AGC basic behavior is shown in Figure 5.

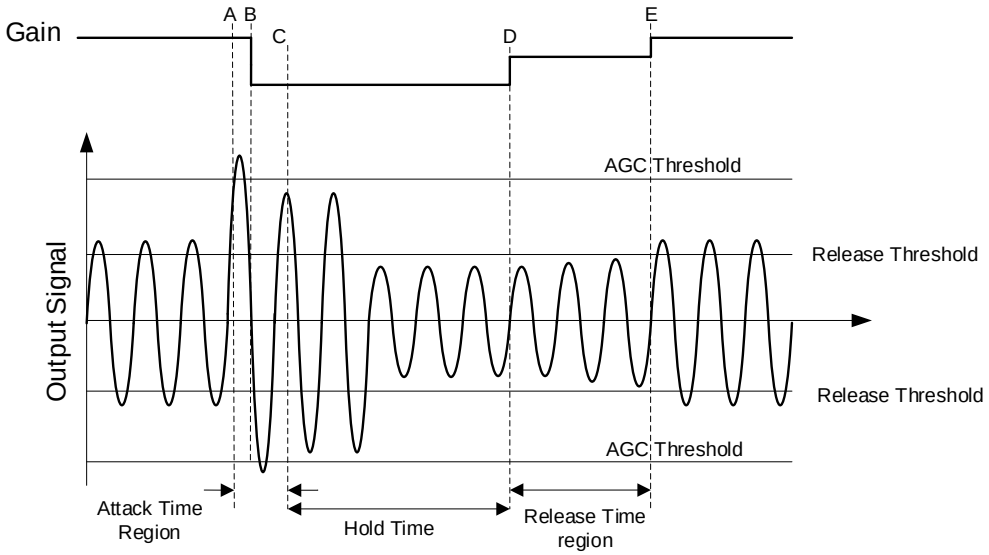


Figure 5, The AGC basic behavior

A. Output signal amplitude is higher than AGC (Limiter, Fast AGC or Slow AGC) threshold, the gain begins to decrease according Attack time setting.
B. Gain decrease occurs at first signal zero crossing after attack time.
C. Attack time ends; Output signal meets target setting.
D. Gain increases after Hold time finishes and signal amplitude remains below desired level.

E. Gain hold after release time is finished again because signal amplitude meets desired level.

The following graphs and explanations show the effect of each variable to the AGC independently and which considerations should be taken when choosing values.

In general, the limiter provides the maximum amplifier output amplitude and it owns shorter compression time then FAST AGC and Slow AGC. All time variables (attack and release) start counting after AGC gain change performed base on register setting. The AGC is allowed to decrease the gain (attack) at first zero-crossing after attack time. The AGC is allowed to increase the gain (release) at first zero-crossing after release time.

The hold time is only enabled after a gain decrease (attack). The hold time replaces the release time after a gain decrease (attack). If the gain needs to be increased further, then the release time is used.

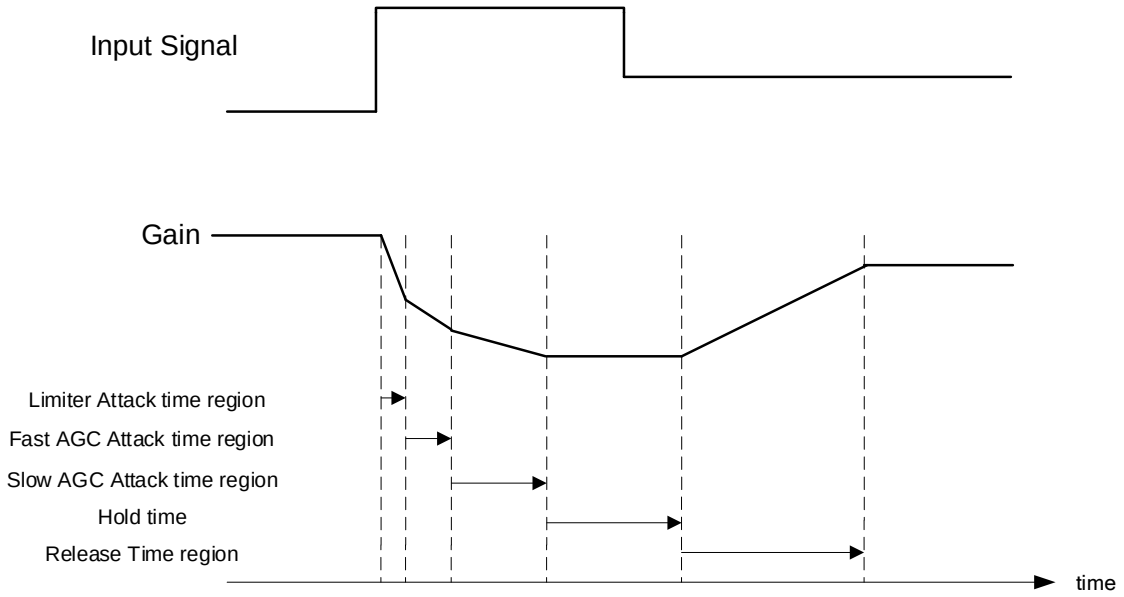


Figure 6, Triple-Level AGC Operation Principle

OCS-Zero adjustment

Traditional AGC doesn't contain OCS-Zero adjustment technology; AGC gain changes generally at the peak, the gain variation at the peak would generate a certain transient distortion, such distortions are audibly imperceptible. Such as individual songs have a slight click

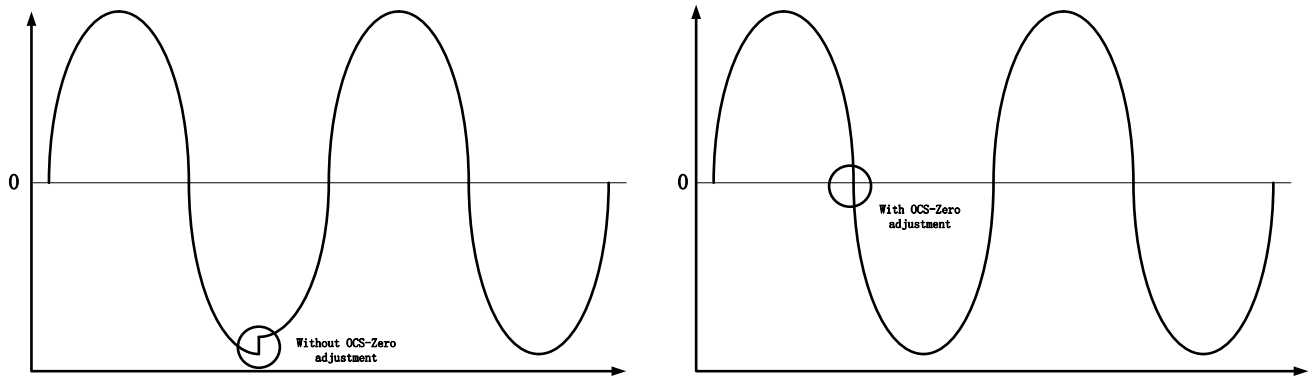


Figure 7, Traditional AGC & OCS-Zero AGC

Adaptive Charge Pump technology

To improve system efficiency during low or middle audio output, adaptive charge pump method is adopted. The charge pump output varies with output level. When PA output power is less than power threshold (P_{TH}), the charge pump is at direct though mode and PVDD is equal to VDD. When PA output power is more than power threshold (P_{TH}), the charge pump is at 2X mode and PVDD is equal to 2*VDD

Speaker & Receiver 2 in 1 application

OCA72390WPAD built-in speaker and receiver 2-in-1 application mode, through the register settings, class D-type 2-in-1 receiver mode gain can be adjusted through the I2C register 0x05, adjustable range of 0~9dB. Speaker and Receiver signal use one signal path together, customers do not need extra component, so the system cost and PCB space are saved.

TDD noise suppression/ Radiation noise suppression

OCA72390WPAD features a unique conduction noise suppression circuit, making the power amplifier to maintain high PSRR value even in the input resistance, the input capacitance deviation of 10% or more, this greatly inhibits the generation of conducted noise.

Over temperature protection

When the chip operates in a fault condition, the chip temperature is too high, up to a preset temperature protection temperature threshold (160°C), the system starts overheating protection, the chip will be turned off, restarts to resume normal work when the chip temperature returns to normal operating range (less than 130°C)

Automatic recovery of overcurrent protection

OCA72390WPAD with automatic recovery of the output overcurrent protection function, when the overcurrent occurs, OCA72390WPAD internal protection circuit will chip off to ensure that the chip is not damaged, when the short-circuit fault is eliminated, the chip will automatically resume working without restarting

■ Device Address

ADDR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AD1 = L & AD2 = L	1	0	1	1	0	0	0	R/W
AD1 = H & AD2 = L	1	0	1	1	0	0	1	R/W
AD1 = L & AD2 = H	1	0	1	1	0	1	0	R/W
AD1 = H & AD2 = H	1	0	1	1	0	1	1	R/W

■ Register Map

ADDR	Register Name	Type	Reset Value	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00H	Device ID	RO	0x11	0	0	0	1	0	0	0	1
01H	System Setting	R/W	0x0C	0	0	0	0	PA_EN	CP_EN	0	CHIP_EN
02H	Mode Setting	R/W	0x0C	0	0	0	ADP_EN	2XCP_EN	SPK_EN	LG_EN	AB_EN
03H	CPOVP	R/W	0x08	0	0	0	0	CP_OUT[3]	CP_OUT[2]	CP_OUT[1]	CP_OUT[0]
04H	CPP	R/W	0x09	0	0	0	0	1	0	0	1
05H	Gain	R/W	0x0C	0	0	0	Gain[4]	Gain[3]	Gain[2]	Gain[1]	Gain[0]
06H	AGC3_Po	R/W	0x07	AGC3_ENN	0	0	0	AGC3_Po[3]	AGC3_Po[2]	AGC3_Po[1]	AGC3_Po[0]
07H	AGC3	R/W	0x4E	AGC3_RT[2]	AGC3_RT[1]	AGC3_RT[0]	AGC3_AT[2]	AGC3_AT[1]	AGC3_AT[0]	AGC3_FAST[1]	AGC3_FAST[0]
08H	AGC2_Po	R/W	0x06	AGC2_ENN	0	0	0	AGC2_Po[3]	AGC2_Po[2]	AGC2_Po[1]	AGC2_Po[0]
09H	AGC2	R/W	0x08	0	0	0	AGC2_AT[2]	AGC2_AT[1]	AGC2_AT[0]	AGC2_FAST[1]	AGC2_FAST[0]
0AH	AGC1	R/W	0x4A	AGC1_ENN	1	0	0	1	AGC1_AT[1]	AGC1_AT[0]	0
0BH	ADP	R/W	0x26	0	0	1	0	ADP_Po[1]	ADP_Po[0]	1	0

DEVICE ID

Address: 00h

Reset Value: 8’b 0001_0001

Type: Read

Bits	Name	Size	Description
[7:6]	Vendor ID	2	Vendor ID
[5:3]	Version ID	3	Device Version ID
[2:0]	Revision ID	3	Revision History ID
Chip ID will be returned after reading. All configuration registers will be reset to default values after 0XAA is written.			

System Setting

Address: 01h

Reset Value: 8’b 0001_0001

Type: Read/Write

Bits	Name	Size	Description
[7:4]	Reserved	4	Do Not Use
3	PA_EN	1	PA Enable/Disable
			0: PA Disable
			1: PA Enable
2	CP_EN	1	Charge pump Enable/Disable
			0: CP Disable
			1: CP Enable, CP operation mode set by ‘2XCP_EN’
1	Reserved	1	Do Not Use
0	CHIP_EN	1	Chip Enable/Disable

			0: Chip Disable
			1: Chip Enable

Mode Setting

Address: 02h

Reset Value: 8'b 0000_1100

Type: Read/Write

Bits	Name	Size	Description
[7:5]	Reserved	3	Do Not Use
4	ADP_EN	1	Adaptive Charge pump function
			0: Adaptive Charge Pump function disable
			1: Adaptive Charge Pump function enable
3	2XCP_EN	1	2X Charge Pump Enable:
			0: Direct Though mode enable
			1: 2X Charge Pump Mode enable
2	SPK_EN	1	Speaker Mode/Receiver Mode
			0: Receiver Mode enable
			1: Speaker Mode enable
1	LG_EN	1	Low Gain Mode
			0: Low Gain Mode Disable
			1: Low Gain Mode Enable
0	AB_EN	1	Class AB path/Class D path:
			0: Class D path enable
			1: Class AB path enable

CPVOUT

Address: 03h

Reset Value: 8'b 0000_1000

Type: Read/Write

Bits	Name	Size	Description
[7:4]	Reserved	4	Do Not Use
[3:0]	CP_VOUT	4	Charge Pump Output Voltage with Class D path (CP_EN=1 && 2XCP_EN=1&&AB_EN=0):
			0000: 6.0V
			0001: 6.25V
			0010: 6.5V
			0011: 6.75V
			0100: 7.0V
			0101: 7.25V
			0110: 7.5V
			0111: 7.75V
			1000: 8.0V
			1001: 8.25V
			1010: 8.5V

			Others: 8.5V
			Charge Pump Output Voltage with Class AB path (CP_EN=1 && 2XCP_EN=1&&AB_EN=1):
			0000: 6.0V
			0001: 6.25V
			0010: 6.5V
			Others: 6.0V

Charge Pump setting

Address: 04h

Reset Value: 8'b 0000_1001

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Reserved	8	Do Not Use

PA Setting

Address: 05h

Reset Value: 8'b 0000_1100

Type: Read/Write

For SPK_EN=1&&LG_EN=1:

Bits	Name	Size	Description
[7:5]	Reserved	3	Do Not Use
[4:0]	PA_GAIN	5	PA Gain Setting 00000: 0dB 00001: 1.5dB 00010: 3dB 00011: 4.5dB 00100: 6dB 00101: 7.5dB 00110: 9dB 00111: 10.5dB 01000: 12dB 01001: 13.5dB 01010: 15dB 01011: 16.5dB 01100: 18dB 01101: 19.5dB 01110: 21dB 01111: 22.5dB 10000: 24dB 10001: 25.5dB 10010: 27dB

For SPK_EN=1&&LG_EN=1

Reset Value: 8'b 0000_0000

Bits	Name	Size	Description
[7:5]	Reserved	3	Do Not Use
[4:0]	PA_GAIN	5	PA Gain Setting 01000: 12dB 01001: 13.5dB 01010: 15dB 01011: 16.5dB 01100: 18dB 01101: 19.5dB 01110: 21dB 01111: 22.5dB 10000: 24dB 10001: 25.5dB 10010: 27dB Others: 24dB

For SPK_EN=0:

Reset Value: 8'b 0000_1100

Bits	Name	Size	Description
[7:5]	Reserved	3	Do Not Use
[4:0]	PA_GAIN	5	PA Gain Setting 00000: 0dB 00001: 1.5dB 00010: 3dB 00011: 4.5dB 00100: 6dB 00101: 7.5dB 00110: 9dB Others: 0dB

Slow AGC Output

Address: 06h

Reset Value: 8'b 0000_0111

Type: Read/Write

For SPK_EN=1&&LG_EN=1

Bits	Name	Size	Description	
7	Slow AGC_ENN	1	Slow AGC Enable/Disable	
			0: Enable	
			1: Disable	
[6:4]	Reserved	3	Do Not Use	
[3:0]	Slow AGC Output Level	4	Slow AGC Output Level	
			0000: 0.1W@8ohm	0000: 0.13W@6ohm
			0001: 0.2W@8ohm	0001: 0.27W@6ohm
			0010: 0.3W@8ohm	0010: 0.40W@6ohm

			0011: 0.4W@8ohm	0011: 0.53W@6ohm
			0100: 0.5W@8ohm	0100: 0.67W@6ohm
			0101: 0.6W@8ohm	0101: 0.80W@6ohm
			0110: 0.7W@8ohm	0110: 0.93W@6ohm
			0111: 0.8W@8ohm	0111: 1.07W@6ohm
			1000: 0.9W@8ohm	1000: 1.20W@6ohm
			1001: 1.0W@8ohm	1001: 1.33W@6ohm
			1010: 1.1W@8ohm	1010: 1.47W@6ohm
			1011: 1.2W@8ohm	1011: 1.60W@6ohm
			1100: 1.3W@8ohm	1100: 1.73W@6ohm
			1101: 1.4W@8ohm	1101: 1.87W@6ohm
			1110: 1.5W@8ohm	1110: 2.0W@6ohm
			1111: 1.6W @8ohm	1111: 2.13W@6ohm

For SPK_EN=1&&LG_EN=0

Bits	Name	Size	Description	
[7:5]	Reserved	3	Do Not Use	
4	Slow AGC_ENN	1	Slow AGC Enable/Disable	
			0: Enable	
			1: Disable	
[3:0]	Slow AGC Output Level	4	Slow AGC Output Level	
			0000: Reserved	0000: Reserved
			0000: Reserved	0000: Reserved
			0000: Reserved	0000: Reserved
			0000: Reserved	0000: Reserved
			0100: 0.5W@8ohm	0100: 0.67W@6ohm
			0101: 0.6W@8ohm	0101: 0.80W@6ohm
			0110: 0.7W@8ohm	0110: 0.93W@6ohm
			0111: 0.8W@8ohm	0111: 1.07W@6ohm
			1000: 0.9W@8ohm	1000: 1.20W@6ohm
			1001: 1.0W@8ohm	1001: 1.33W@6ohm
			1010: 1.1W@8ohm	1010: 1.47W@6ohm
			1011: 1.2W@8ohm	1011: 1.60W@6ohm
			1100: 1.3W@8ohm	1100: 1.73W@6ohm
			1101: 1.4W@8ohm	1101: 1.87W@6ohm
			1110: 1.5W@8ohm	1110: 2.0W@6ohm
			1111: 1.6W @8ohm	1111: 2.0W@6ohm

For SPK_EN=0

Bits	Name	Size	Description
7	Slow AGC_ENN	1	Slow AGC Enable/Disable
			0: Enable
			1: Disable
[6:4]	Reserved	3	Do Not Use
[3:0]	Slow AGC Output Level	4	Slow AGC Output Level

			0000~1111: AGC3 Off

Slow AGC Control

Address: 07h

Reset Value: 8'b 0100_1110

Type: Read/Write

Bits	Name	Size	Description
[7:5]	Slow AGC Release Time	3	000: 5.12ms/dB
			001: 10.24ms/dB
			010: 20.48ms/dB
			011: 40.96ms/dB
			100: 81.92ms/dB
			101: 163.84ms/dB
			110: 327.68ms/dB
			111: 655.36ms/dB
[4:2]	Slow AGC Attack Time	3	000: 1.28ms/dB
			001: 2.56ms/dB
			010: 10.24ms/dB
			011: 40.96ms/dB
			100: 81.92ms/dB
			101: 163.84ms/dB
			110: 327.68ms/dB
			111: 655.36ms/dB
[1:0]	Slow AGC First Attack Time	2	00: 10.24ms/dB
			01: 20.48ms/dB
			10: 40.96ms/dB
			11: 81.92ms/dB

Fast AGC Output

Address: 08h

Reset Value: 8'b 0000_0110

Type: Read/Write

For SPK_EN=1

Bits	Name	Size	Description	
7	Fast AGC_ENN	1	Fast AGC Enable/Disable	
			0: Enable	
			1: Disable	
[6:4]	Reserved	4	Do Not Use	
[3:0]	Fast AGC Output Level	4	0000: 0.4W@8ohm	0000: 0.53W@6ohm
			0001: 0.6W@8ohm	0001: 0.80W@6ohm
			0010: 0.8W@8ohm	0010: 1.06W@6ohm
			0011: 1.0W@8ohm	0011: 1.33W@6ohm
			0100: 1.2W@8ohm	0100: 1.60W@6ohm
			0101: 1.4W@8ohm	0101: 1.87W@6ohm

			0110: 1.6W@8ohm	0110: 2.17W@6ohm
			0111: 1.8W@8ohm	0111: 2.40W@6ohm
			1000: 2.0W@8ohm	1000: 2.67W@6ohm
			Others: 1.6W@8ohm	Others: 2.17W@6ohm

For SPK_EN=0

Bits	Name	Size	Description
7	Fast AGC_ENN	1	Fast AGC Enable/Disable
			0: Enable
			1: Disable
[6:4]	Reserved	4	Do Not Use
[3:0]	Fast AGC Output Level	4	0000~1111: Fast AGC Off

Fast AGC Control

Address: 09h

Reset Value: 8'b 0000_1000

Type: Read/Write

Bits	Name	Size	Description
[7:5]	Reserved	3	Do Not Use
[4:2]	Fast AGC Attack Time	3	000: 0.16ms/dB
			001: 0.32ms/dB
			010: 0.64ms/dB
			011: 2.56ms/dB
			100: 10.24ms/dB
			101: 40.96ms/dB
			110: 82ms/dB
			111: 164ms/dB
[1:0]	Fast AGC First Attack Time	2	00: 0.16ms/dB
			01: 0.64ms/dB
			10: 2.56ms/dB
			11: 10.24ms/dB

Limiter Control

Address: 0Ah

Reset Value: 8'b 0100_1010

Type: Read/Write

Bits	Name	Size	Description
7	Limiter_ENN	1	Limiter Enable/Disable
			0: Enable
			1: Disable
[6:3]	Reserved	5	Do Not Use
[2:1]	Limiter Attack Time	2	00: 0.04ms/dB
			01: 0.08ms/dB
			10: 0.16ms/dB
			11: 0.32ms/dB

0	Reserved	1	Do Not Use

Adaptive Charge Pump Setting

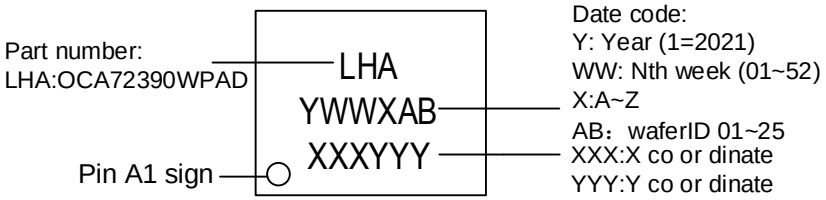
Address: 0Bh

Reset Value: 8'b 0010_0110

Type: Read/Write

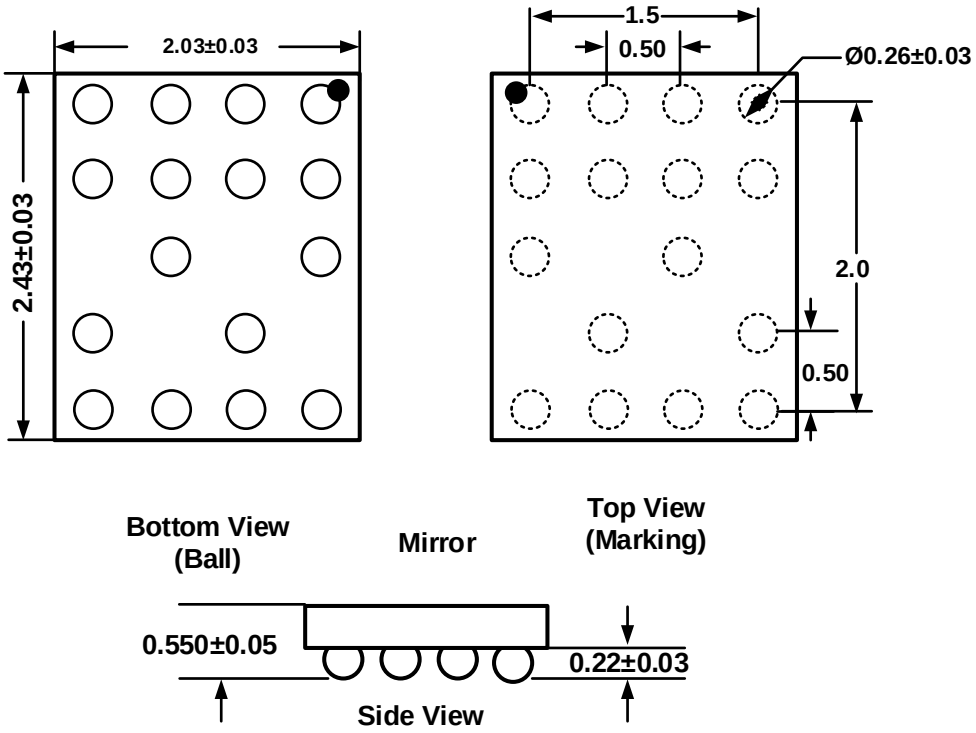
Bits	Name	Size	Description
[7:4]	Reserved	4	Do Not Use
[3:2]	ADP CP_LEVEL Threshold SETTING	2	00: 0.1W
			01: 0.2W
			10: 0.3W
			11: 0.4W
[1:0]	Reserved	2	Do Not Use

■ Marking Information

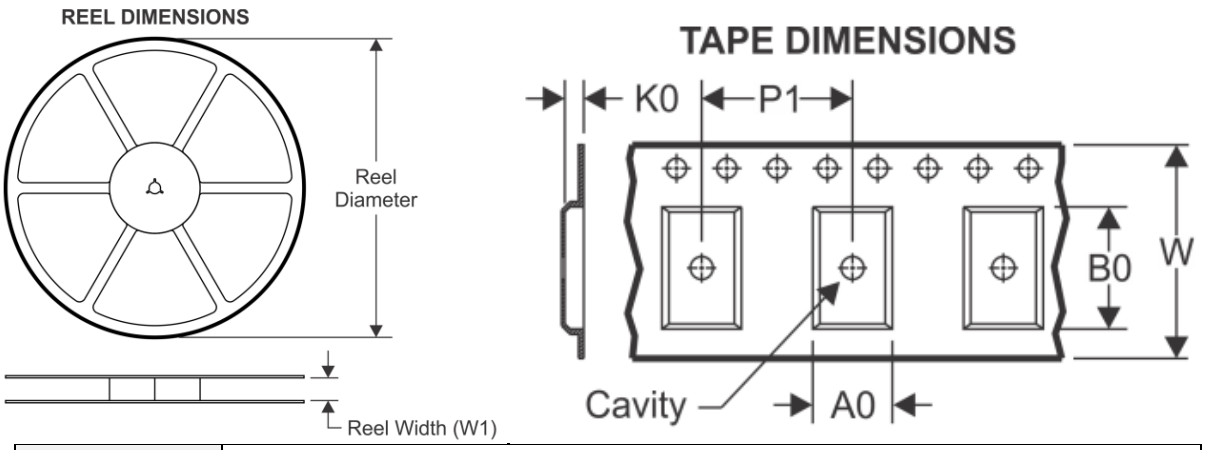


■ Package Information

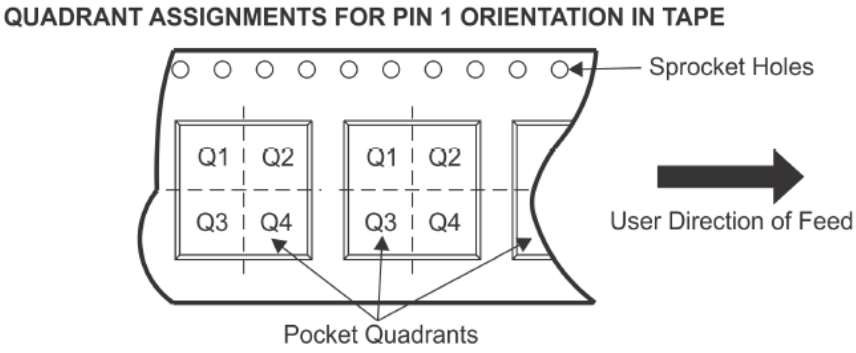
WLCSP-16B



■ Packing Information



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Package tape	Package Drawing	MSL	SPQ	Reel Diameter (mm)	Reel Width W1(mm)
WLCSP-16B	LHA	Level-1-260C	3000PCS	180	8.4
A0 (mm)	**B0 (mm)**	**K0 (mm)**	**P1 (mm)**	**W (mm)**	**PIN A1 Quadrant**
2.15	2.55	0.75	4.0	8.0	Q1

IMPORTANT NOTICE

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