■ General Description

OCH1970VAD-H is a high accuracy 16 bit data out for 3D magnetic sensor IC with high sensitivity and wide measurement range utilizing our latest Hall sensor technology.

Our ultra-small package of OCH1970VAD-H incorporates magnetic sensors, chopper stabilized signal, amplifier chain, and all necessary interface logic for detecting weak to strong magnetic fields in the X, Y and Z planes independently. From its compact foot print, thin package, and extremely low power consumption, it is suitable for a wide range of applications such as connected home, door & window opening/close sensing, and magnetic tamper detection of IoT systems or smart meters just to name a few.

The OCH1970VAD-H is available in 8-pin DFN package and is rated over the -40℃ to 85℃.

■ Features

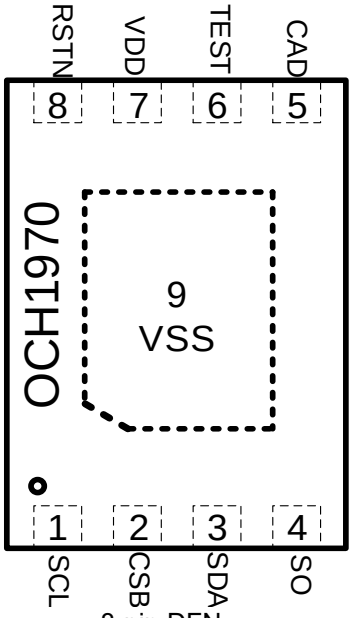
- Operating supply voltage: +1.7V to +3.6V
- Operating temperatures: -40℃~+85℃
- 16 bit data out for each 3-axis magnetic component
- Built-in A to D Converter for magnetometer data output
- Selectable sensor measurement range and sensitivity setting:
  ★High sensitivity setting
  Sensitivity: 1.1 μT/LSB (typ.)
  Measurement range: ± 36 mT
  ★Wide range setting
  Sensitivity: 3.1 μT/LSB (typ.)
  Measurement range: X and Y-axis → ±34.9mT, Z-axis → ±101.5mT
- Serial interface:
  ★I2C bus interface
  ★4-wire SPI
- Operation mode:
  ★Power-down
  ★Single measurement
  ★Continuous measurement
- DRDY function for measurement data ready
- Magnetic sensor overflow monitor function
- Selectable sensor drive:
  ★Low power drive / Low noise drive
- Package:
  ★8-Pin DFN: 2.0mm x 3.0mm x 0.55mm
- RoHS Compliant

■ Applications

- Position Detection
- Home appliances

■ Pin Configuration

(Top View)



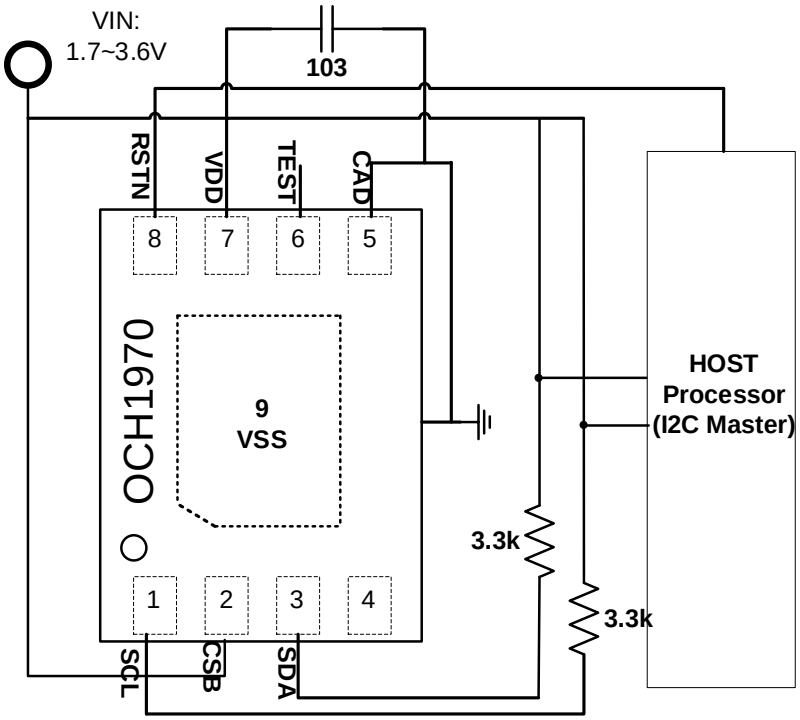
8-pin DFN

Figure 1, Pin Assignments Of OCH1970VAD-H

Pin Name	Pin Number 8-pin DFN	Pin Function
SCL	1	When the I2C bus interface is selected (CSB pin is connected to VDD). SCL: Control clock input pin Input: Schmitt trigger
SK		When the 4-wire SPI is selected. SK: Serial clock input pin
CSB	2	Chip select pin for 4-wire SPI “L” active. Connect to VDD when selecting I2C bus interface.
SDA	3	When the I2C bus interface is selected (CSB pin is connected to VDD). SDA: Control data input/output pin Input: Schmitt trigger, Output: Open-drain
SI		When the 4-wire SPI is selected. SI: Serial data input pin
SO	4	When the I2C bus interface is selected (CSB pin is connected to VDD) Hi-Z output. Keep this pin electrically non-connected.
		When the 4-wire SPI is selected. Serial data output pin
CAD	5	When the I2C bus interface is selected (CSB pin is connected to VDD). CAD: Slave address input pin Connect to VSS or VDD.
		When the 4-wire serial interface is selected. Connect to VSS
TEST	6	Test and Factory Calibration
VDD	7	Positive power supply pin
RSTN	8	Reset pin Resets registers by setting to “L”.
VSS	9	Ground pin

■ Typical Application Circuit

I2C bus interface:



4-wire SPI:

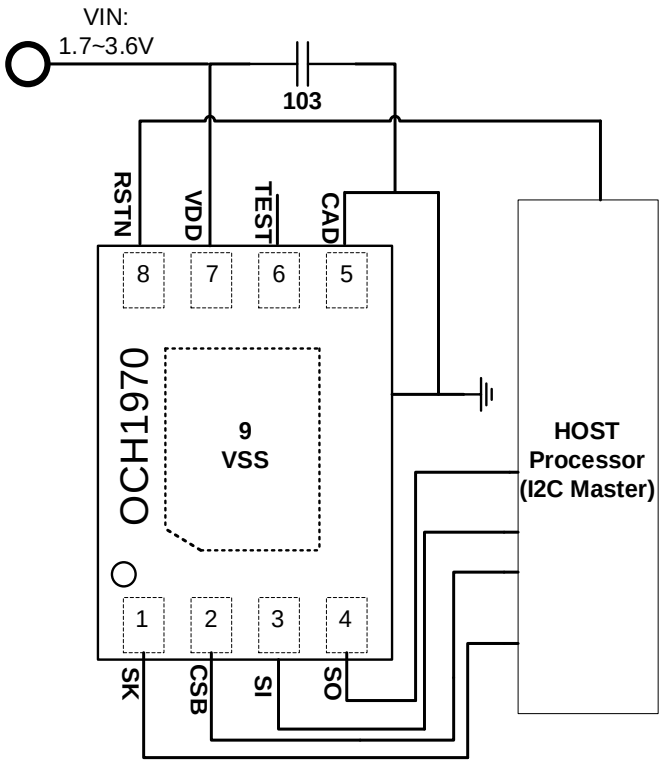


Figure 2, Typical Application Circuit of OCH1970VAD-H

■ Ordering Information

PartNumber	Package Type	Packing Qty.	Temperature	Eco Plan	Lead
OCH1970VAD-H	DFN-8L	3000	-40~ +85℃	ROHS	Cu

■ Block Diagram

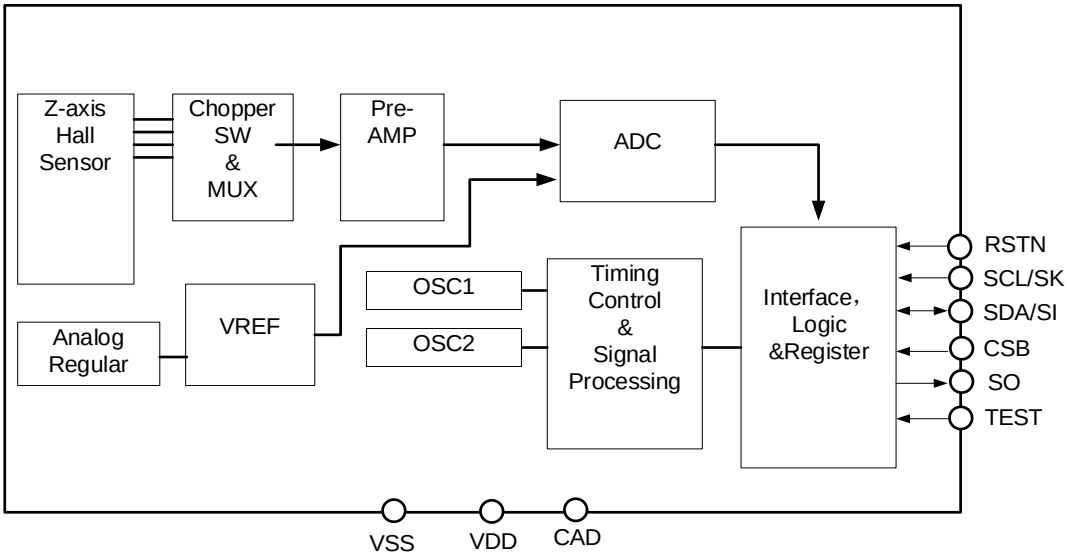


Figure 3, Block Diagram Of OCH1970VAD-H

■ Absolute Maximum Ratings[1] (T_A=25°C, unless otherwise noted)

Parameter		Symbol	Rating	Unit
V_{DD} Pin to GND		V_{DD}	-0.3~+4.3	V
Input voltage		V_{IN}	-0.3~V_{DD}+0.3	V
Input current		I_{IN}	-10~+10mA	mA
Junction temperature		T_J	150	℃
Continuous power dissipation(T_A=+25℃)	8-pin DFN	Pd	1.3	W
Thermal Resistance	8-pin DFN	θJA	95	℃/W
Storage Temperature Range		T_S	-55 to +150	℃
Operating Junction Temperature Range		T_J	-40 to +150	℃
Maximum Soldering Temperature (at leads, 10 sec)		T_{LEAD}	260	℃

■ Recommended Operating Conditions[2]

Parameter	Symbol	Rating	Unit
V_{DD} Pin Voltage to GND	V_{DD}	1.7 to 3.6	V
Operating junction Temperature Range	T_{OP}	-40 to +85	℃

Note: 1: Stresses above those listed in absolute maximum ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one absolute maximum rating should be applied at any one time.

2: The device is not guaranteed to function outside of its operating conditions.

■ Electrical Characteristics

The following conditions apply unless otherwise noted: Vdd = 1.7V to 3.6V, Temperature range = -40~+85℃,
Typical condition: V_{DD} = 1.8 V, Temperature = 25 ℃。

DC Characteristics

Parameter	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
High level input voltage	VIH	CSB RSTN SCL/SK SDA/SI CAD	-	70%V_{DD}	-	-	V
Low level input voltage	VIL		-	-	-	30%V_{DD}	V
Input current	IIN		VIN=VSS or VDD	-10	-	+10	uA
Hysteresis input voltage [1]	VHS	CSB RSTN SCL/SK SDA/SI	VDD≥2V	5%V_{DD}	-	-	V
			VDD＜2V	10%V_{DD}	-	-	
High level output voltage [2]	VOH	SO	IOH≥-100μA	80%V_{DD}	-	-	V
Low level output voltage 1 [2]	VOL1	SO	IOL≤+100μA	-	-	20%V_{DD}	V
Low level output voltage 2 [3]	VOL2	SDA/SI	IOL2≤+3mA VDD≥2V	-	-	0.4	V
			IOL2≤+3mA VDD＜2V	-	-	20%V_{DD}	V
Current consumption [4]	IDD1	VDD	Power-down mode	-	8.6	16	μA
	IDD2		When magnetic sensor is driven		1.9	2.5	mA
	IDD3		All Power-down (RSTN pin = L)		8.6	16	μA

Notes:
1. Schmitt trigger input (reference value for design).
2. IOH: High level output current. IOL: Low level output current.
3. Output is open-drain. Connect to a pull-up resistor externally.
4. Without any resistance load.

AC Characteristics of RSTN

Parameter	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
Wait time for reset	twRST	RSTN	V_{DD} > 80%V_{DD}	5	-	-	us
Reset input effective pulse width	tRSTL		V_{DD} > 80%V_{DD}	5	-	-	us
Reset input ineffective pulse width	tSPRST		-	-	-	1	us

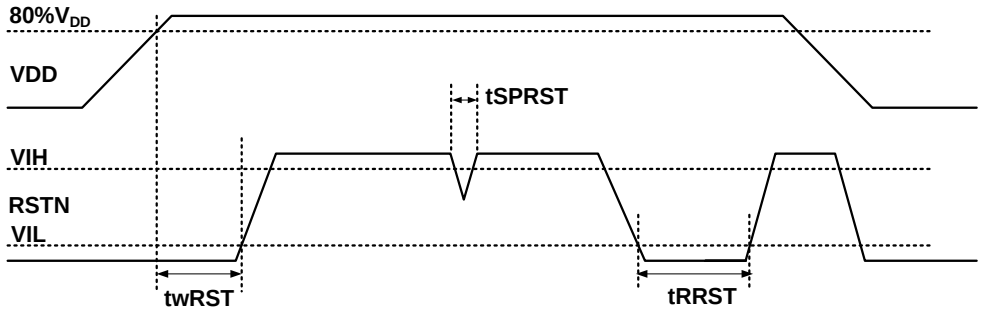


Figure 4, Reset condition

■ Overall Characteristics

Table 8.1 High sensitivity setting

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Measurement data output bit	DBIT	-	-	16	-	Bit
Time for measurement	TSM	SDR bit = “0” (Low noise drive)	-	0.792	0.872	ms
		SDR bit = “1” (Low power drive)	-	0.31	0.341	
Magnetic sensor sensitivity	BSE	Ta=25℃, SMR bit = “0”	0.99	1.1	1.21	μT/LSB
Magnetic sensor measurement range	BRG	Ta=25℃, SMR bit = “0”	±32.44	±36.04	±39.64	mT
Magnetic sensor initial offset* [5]	BOF	Ta=25℃ X and Y-axis	-614	-	+614	LSB
		Ta=25℃ Z-axis	-868	-	+868	
Noise* [6]	NIS	SDR bit = “0” (Low noise drive)	-	9.7	-	μTrms
		SDR bit = “1” (Low power drive)	-	19.5	-	

Table 8.2 Wide range setting

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Measurement data output bit	DBIT	-	-	16	-	Bit
Time for measurement	TSM	SDR bit = “0” (Low noise drive)	-	0.792	0.872	ms
		SDR bit = “0” (Low power drive)	-	0.31	0.341	
Magnetic sensor sensitivity	BSE	Ta=25℃, SMR bit = “1”	2.79	3.1	3.41	μT/LSB
Magnetic sensor measurement range	BRG	Ta=25℃ X and Y-axis, SMR bit = “1”	±31.42	±34.91	±38.4	mT
		Ta=25℃ Z-axis, SMR bit = “1”	±91.42	±101.57	±111.73	
Magnetic sensor initial offset* [5]	BOF	Ta=25℃ X and Y-axis	-218	-	+218	LSB
		Ta=25℃ Z-axis	-308	-	+308	
Noise* [6]	NIS	SDR bit = “0” (Low noise drive)	-	11.8	-	μTrms
		SDR bit = “1” (Low power drive)	-	23.9	-	

Note:
* 5. Value of measurement data register on shipment test without applying magnetic field on purpose.
* 6. Reference value for design. Under steady magnetic field

4-wire SPI

4-wire SPI is compliant with mode 3 (SPI-mode3)

Parameter		Symbol	Conditions	Min.	Typ.	Max.	Unit
SK clock frequency		Fspi	-	-	-	4.0	MHz
CSB setup time		Tcs	-	50	-	-	ns
Data setup time		Ts	-	50	-	-	ns
Data hold time		Th	-	50	-	-	ns
SK high time		Twh	Vdd≥2.5V	100	-	-	ns
			2.5V>Vdd≥1.7V	150	-	-	ns
SK low time		Twl	Vdd≥2.5V	100	-	-	ns
			2.5V>Vdd≥1.7V	150	-	-	ns
SK setup time		Tsd	-	50	-	-	ns
SK to SO delay time* [7]		Tdd	-	-	-	50	ns
CSB to SO delay time* [7]		Tcd	-	-	-	50	ns
SK rise time* [8]		Tr	-	-	-	100	ns
SK fall time* [8]		Tf	-	-	-	100	ns
CSB high time		Tch	-	450	-	-	ns

Notes:
* 7.SO load capacitance: 20pF.
* 8.Reference value for design.

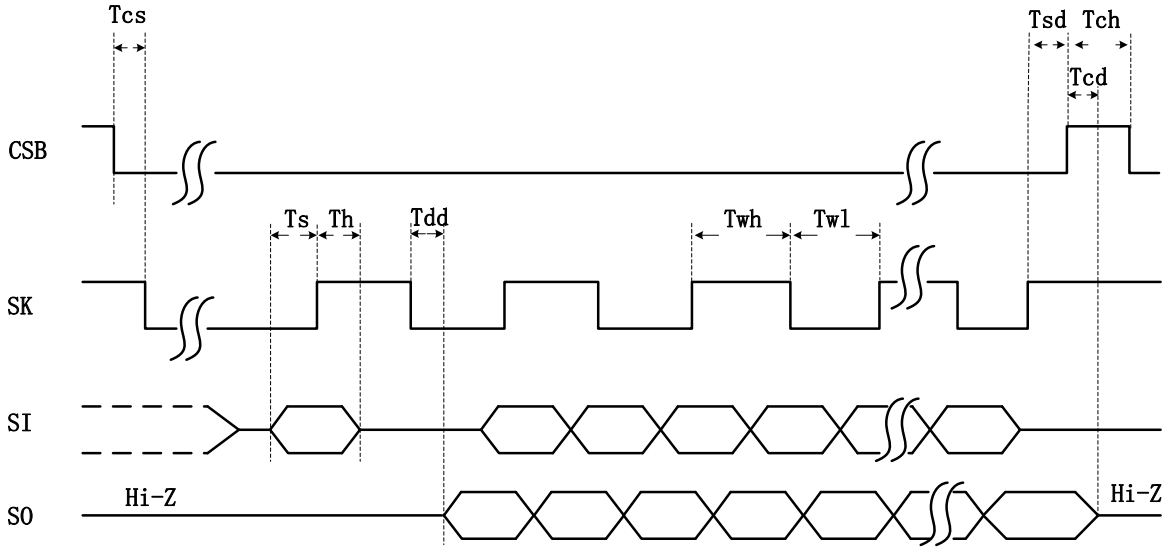


Figure 5, 4-wire SPI

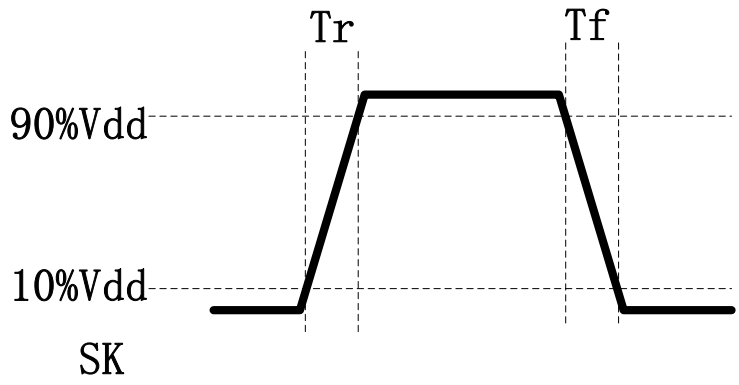


Figure 6, Rise time and fall time

I2C Bus Interface

CSB pin = “H”

I2C bus interface is compliant with Standard mode and Fast mode. Standard/Fast is selected automatically by fSCL.

Table 8.3 Standard mode (fSCL≤100 kHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
SCL clock frequency	fSCL	-	-	-	100	kHz
SCL clock “High” time	tHIGH	-	4.0	-	-	us
SCL clock “Low” time	tLOW	-	4.7	-	-	us
SDA and SCL rise time	tR	-	-	-	1000	ns
SDA and SCL fall time	tF		-	-	300	ns
Start Condition hold time	tHD:STA	-	4.0	-	-	us
Start Condition setup time	tSU:STA	-	4.7	-	-	us
SDA hold time (vs. SCL falling edge)	tHD:DAT	-	0.05	-	3.45	us
SDA setup time (vs. SCL rising edge)	tSU:DAT	-	0.25	-	-	us
Stop Condition setup time	tSU:STO	-	4.0	-	-	us
Bus free time	tBUF	-	4.7	-	-	us
Capacitive load for SCL and SDA	C_B		-	-	0.4	nF

Table 8.4 Fast mode (100 kHz ＜fSCL≤400 kHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
SCL clock frequency	fSCL	-	-	-	400	kHz
SCL clock “High” time	tHIGH	-	0.6	-	-	us
SCL clock “Low” time	tLOW	-	1.3	-	-	us
SDA and SCL rise time	tR	-	-	-	300	ns
SDA and SCL fall time	tF		-	-	300	ns
Start Condition hold time	tHD:STA	-	0.6	-	-	us
Start Condition setup time	tSU:STA	-	0.6	-	-	us
SDA hold time (vs. SCL falling edge)	tHD:DAT	-	0.05	-	0.9	us
SDA setup time (vs. SCL rising edge)	tSU:DAT	-	0.1	-	-	us
Stop Condition setup time	tSU:STO	-	0.6	-	-	us
Bus free time	tBUF	-	1.3	-	-	us
Noise suppression pulse width	tSP	-	-	-	50	ns
Capacitive load for SCL and SDA	C_B	-	-	-	0.4	nF

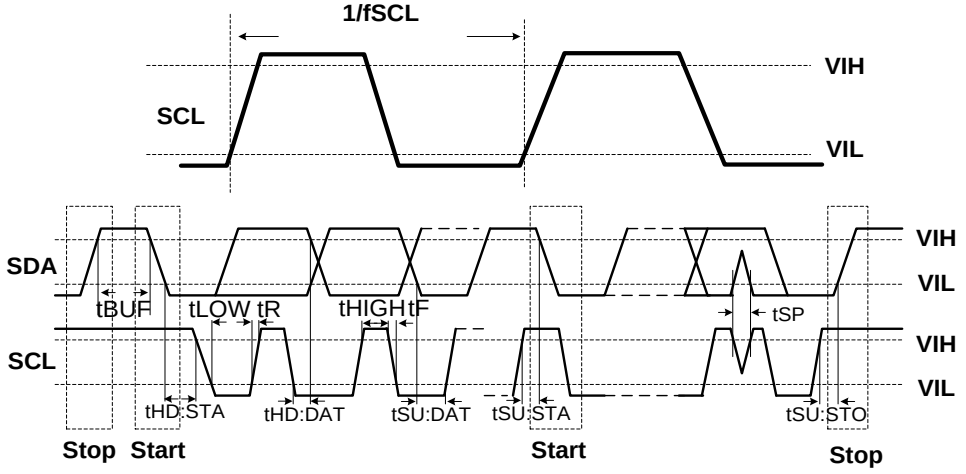


Figure 7, I2C bus interface timing

■ State Transition Diagram

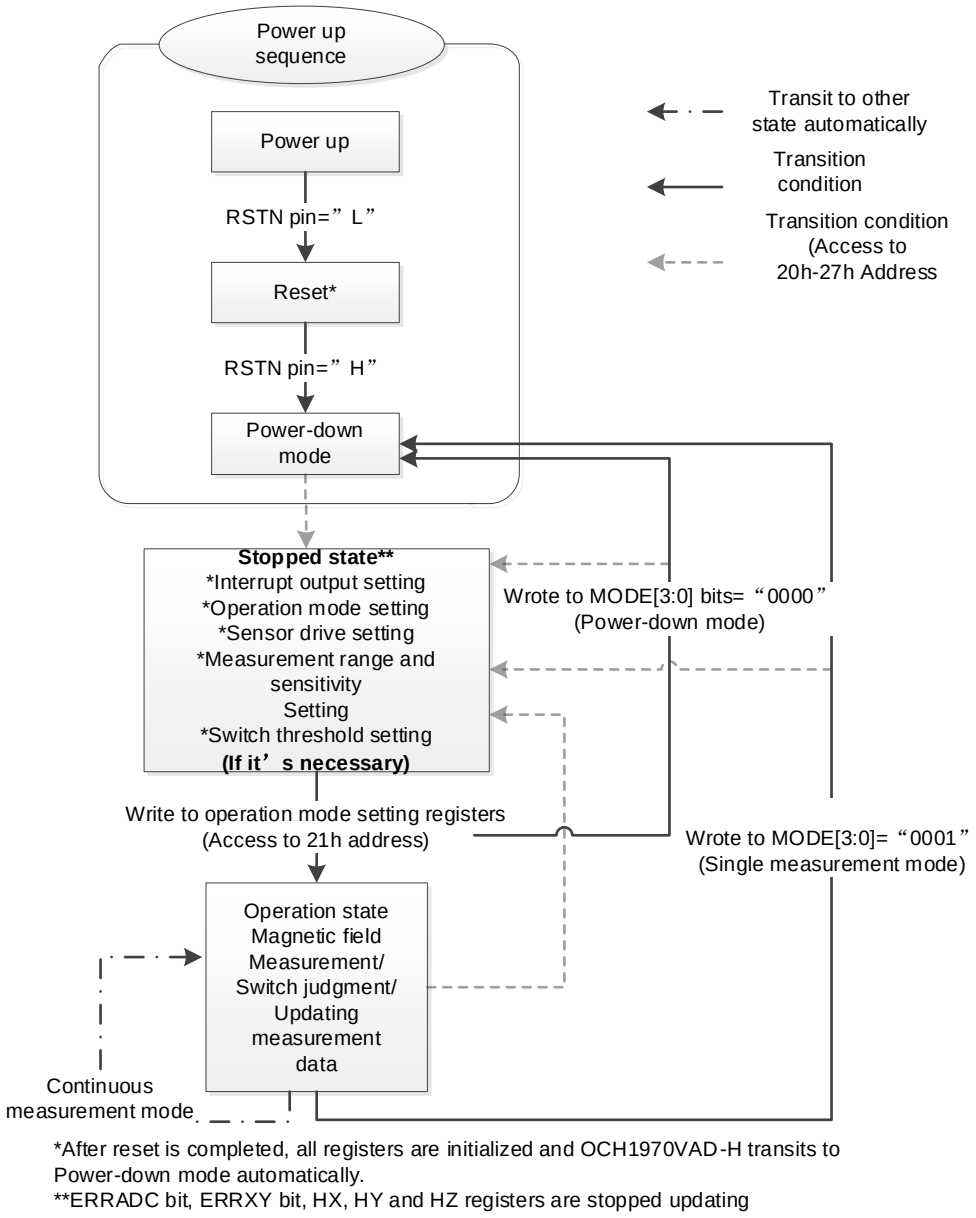


Figure 8 State transition diagram

■ Power States

OCH1970VAD-H does not have built in power on reset circuit. Reset has to be done manually by user. When RSTN pin is applied a specified voltage(VIL), all registers in OCH1970VAD-H are initialized.

Table 9.1Power States

State	VDD	Power state
1	OFF (0V)	OFF (0V). It doesn't affect external interface. Digital input pins other than SCL and SDA should be fixed to "L" (0V).
2	1.7V to 3.6V	ON After reset (RSTN pin = "L"), OCH1970VAD-H can measure magnetic field. Refer to 8.2.

■ Register States

Refer to Figure 8

State	DRDY bit /DOR bit	Measurement data register* [9]	Other register
Reset	0	Default value	Default value
Power-down mode	Refer to 10.3	Default value or previous measurement value	Setting value
Stopped state	DRDY: 0 DOR: previous measurement	Default value or previous measurement value	Setting value
Operation state: (Magnetic field measurement)	Refer to 10.3	Default value or previous measurement value	Setting value
Operation state: (updating measurement data)	Refer to 10.3	Previous measurement value	Setting value

Note:
* 9. HX, HY and HZ registers.

■ Pin States

Refer to Figure 8

State	SDA/SI pin	SO pin	RSTN pin	Other pins
Reset	Hi-Z	Hi-Z	L	Don't care
Power-down mode	Serial interface	Serial interface	H	Don't care
Stopped state	Serial interface	Serial interface	H	Don't care
Operation state: (Magnetic field measurement)	Serial interface	Serial interface	H	Don't care
Operation state: (updating measurement data)	Serial interface	Serial interface	H	Don't care

■ Reset Functions

When OCH1970VAD-H changes to reset status, it consumes the current of reset state (IDD3).

OCH1970VAD-H has two types of reset;

I. Reset pin (RSTN)
   OCH1970VAD-H is reset by Reset pin.
II. Soft reset
   OCH1970VAD-H is reset by setting SRST bit.

Note：

After reset is completed, all registers are initialized and OCH1970VAD-H transits to Power-down mode automatically.

■ Operation modes

OCH1970VAD-H has following nine operation modes:

(1) Power-down mode (MODE[3:0] bits = ”0000”)
(2) Single measurement mode (MODE[3:0] bits = ”0001”)
   - Sensor is measured for one time and data is output. Transits to Power-down mode automatically after measurement ended.

(3) Continuous measurement mode 1 (MODE[3:0] bits = ”0010”)
   - Sensor is measured periodically in 0.5 Hz. Transits to other operation mode by writing MODE[3:0] bits directly.

(4) Continuous measurement mode 2 (MODE[3:0] bits = ”0100”)
   - Sensor is measured periodically in 1 Hz. Transits to other operation mode by writing MODE[3:0] bits directly.

(5) Continuous measurement mode 3 (MODE[3:0] bits = ”0110”)
   - Sensor is measured periodically in 2 Hz. Transits to other operation mode by writing MODE[3:0] bits directly.

(6) Continuous measurement mode 4 (MODE[3:0] bits = ”1000”)
   - Sensor is measured periodically in 20 Hz. Transits to other operation mode by writing MODE[3:0] bits directly.

(7) Continuous measurement mode 5 (MODE[3:0] bits = ”1010”)
   - Sensor is measured periodically in 40 Hz. Transits to other operation mode by writing MODE[3:0] bits directly.

(8) Continuous measurement mode 6 (MODE[3:0] bits = ”1100”)
   - Sensor is measured periodically in 100 Hz. Transits to other operation mode by writing MODE[3:0] bits directly.

(9) Continuous measurement mode 7 (MODE[3:0] bits = ”1110”)
   - Sensor is measured periodically in 500 Hz. Transits to other operation mode by writing MODE[3:0] bits directly.

By setting CNTL2 registers MODE[3:0] bits, the operation set for each mode is started.
When power is turned ON and reset action, OCH1970VAD-H is in Power-down mode. When a specified value is set to MODE[3:0] bits, OCH1970VAD-H transits to the specified mode and starts operation.

■ Description of Each Operation Mode

Power-down Mode

Power to almost all internal circuits is turned off, all registers are accessible in Power-down mode and data stored in read/write registers still remains. They can be reset by soft reset function.

Single Measurement Mode

When Single measurement mode (MODE[3:0] bits = “0001”) is set, magnetic sensor measurement is started. After magnetic sensor measurement and signal processing is finished, measurement magnetic data is stored to measurement data registers(HX, HY and HZ registers), then OCH1970VAD-H transits to Power-down mode automatically. On transition to Power-down mode, MODE[3:0] bits turns to “0000”. At the same time, DRDY bit in ST register turns to “1”

Continuous Measurement Mode 1,2,3,4,5,6 and 7

When Continuous measurement modes (1 to 7) are set, magnetic sensor measurement is started periodically at 0.5Hz, 1 Hz, 2 Hz, 20 Hz, 40 Hz, 100 Hz and 500Hz respectively. After magnetic sensor measurement and signal processing is finished, measurement magnetic data is stored to measurement data registers and all circuits except for the minimum circuit required for counting cycle length are turned off (Power Save: PS). When the next measurement timing comes, OCH1970VAD-H wakes up automatically from PS and starts measurement again. Continuous measurement mode ends when a different operation mode is set or threshold value is reset. It repeats measurement until other operation mode is set or threshold value is reset. When user access to Setting Registers (address 20h to 27h), OCH1970VAD-H stops updating measurement data registers. After CNTL2 register (address 21h) is set again, a new measurement starts. ST register (without DRDY bit and DOR bit) and measurement data registers will not be initialized by this.

Table 10.1 Continuous measurement modes

Operation mode	Register setting (MODE[3:0] bits)	Measurement frequency [Hz]
Continuous measurement mode 1	0010	0.5
Continuous measurement mode 2	0100	1
Continuous measurement mode 3	0110	2
Continuous measurement mode 4	1000	20
Continuous measurement mode 5	1010	40
Continuous measurement mode 6	1100	100
Continuous measurement mode 7	1110	500

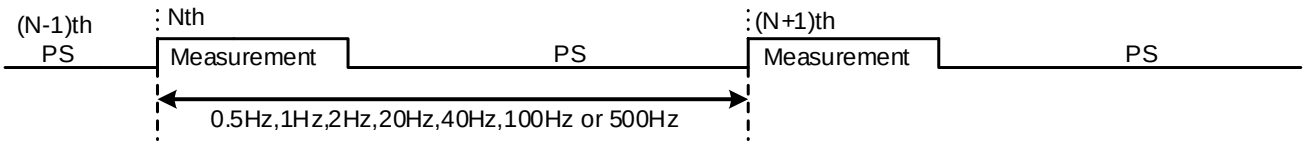


Figure 10.1 Continuous measurement modes

■ Data Ready

When measurement data is stored and ready to be read, DRDY bit in ST1 register turns to “1”. This is called “Data Ready”. When any of measurement data register (HX, HY or/and HZ register) is read all the way through or access to Setting Registers (address 20h to 27h), DRDY bit turns to “0”. Refer to 9.1, 9.3 and 9.4. When measurement is performed correctly, OCH1970VAD-H becomes Data Ready on transition to PS after measurement.

Normal Measurement Data Read Sequence

(1) Check Data Ready or not by any of the following method.
Polling DRDY bit of ST register
When Data Ready, proceed to the next step.

(2) Read ST and measurement data
When ST register and any of measurement data register (HX, HY or/and HZ register) is read all the way through, or access to Setting Registers (address 20h to 27h), OCH1970VAD-H judges that data reading is finished.
When data reading is finished, DRDY bit and DOR bit turns to “0”

When measurement data register is accessed, OCH1970VAD-H judges that data reading is started. Stored measurement data is protected during data reading and data is not updated. By reading measurement data register is finished, this protection is released.

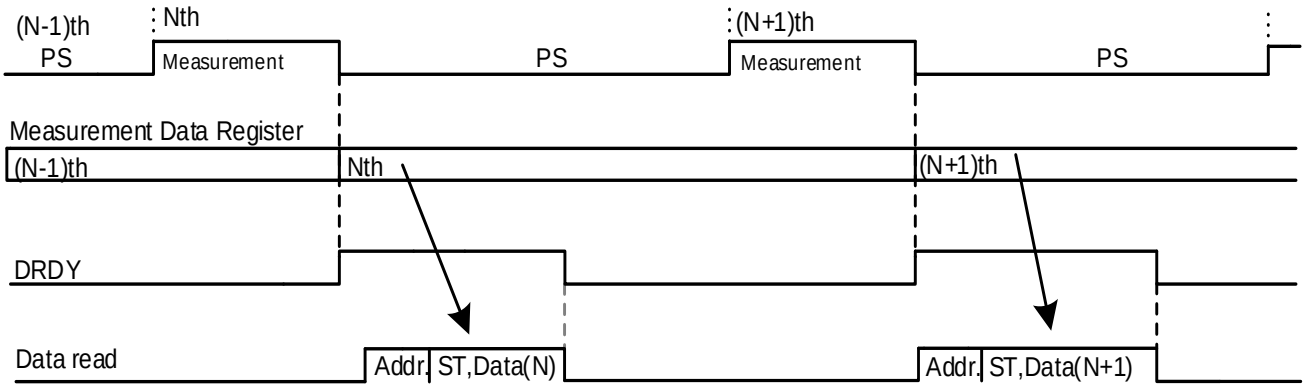


Figure 10.2 Timing chart of Measurement data read

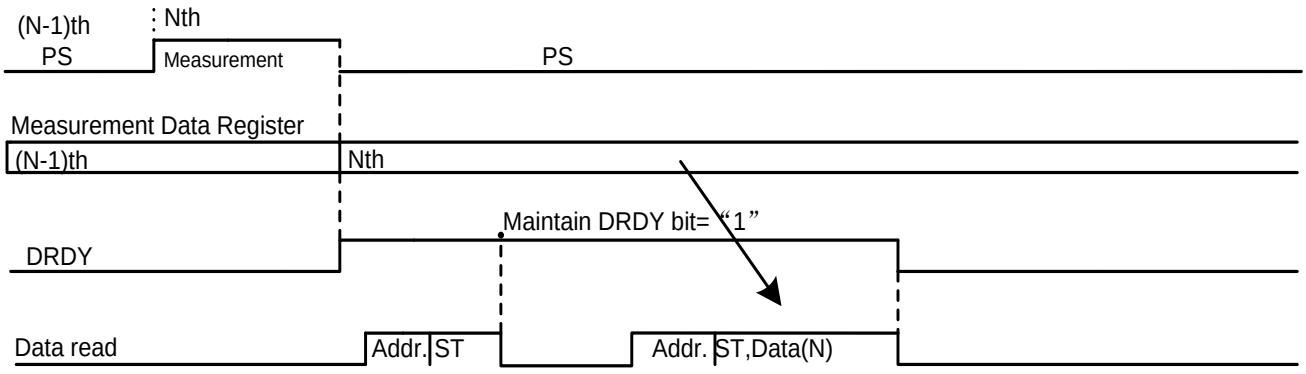


Figure 10.3 Timing chart of ST data read

Data Read Start during Measurement

When the sensor is measuring (Measurement period), measurement data registers (HX, HY and HZ) keep the previous data. Therefore, it is possible to read out data even during the in measurement period. If data is started to be read during measurement period, previous data is read.

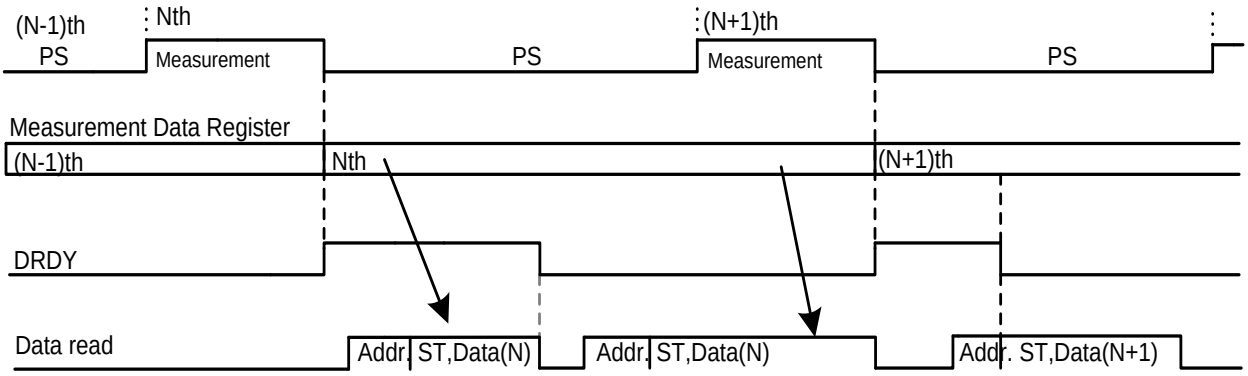


Figure 10.4 Data read start during measuring

Data Skip

When Nth data was not read before (N+1)th measurement ends, Data Ready remains until data is read. In this case, a set of measurement data is skipped so that DOR bit turns to “1”. DOR bit turns to “0” at the (N+2)th measurement ended.

When data reading started after Nth measurement ended and did not finish reading before (N+1)th measurement ended, Nth measurement data is protected to keep correct data. In this case, a set of measurement data is not skipped and stored after finish reading Nth measurement data so that DOR bit=”0”.

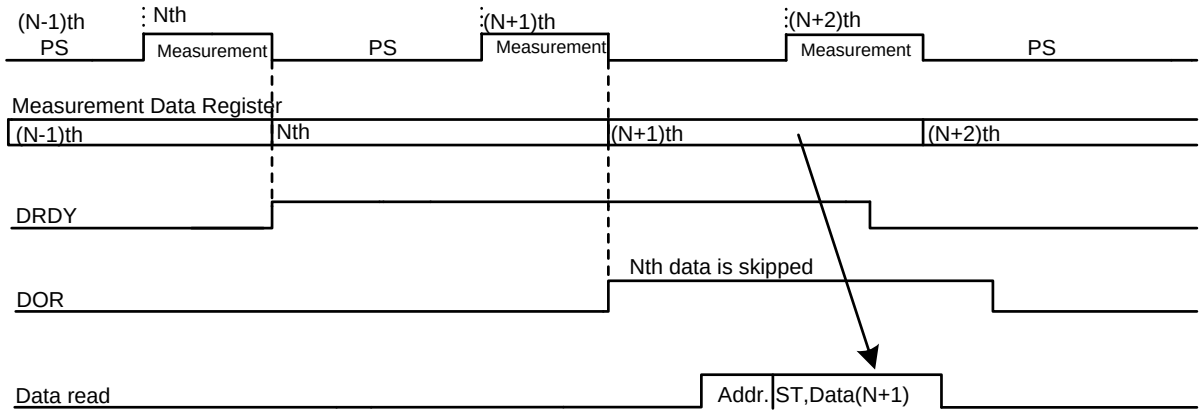


Figure 10.5 Data Skip: When data is not read

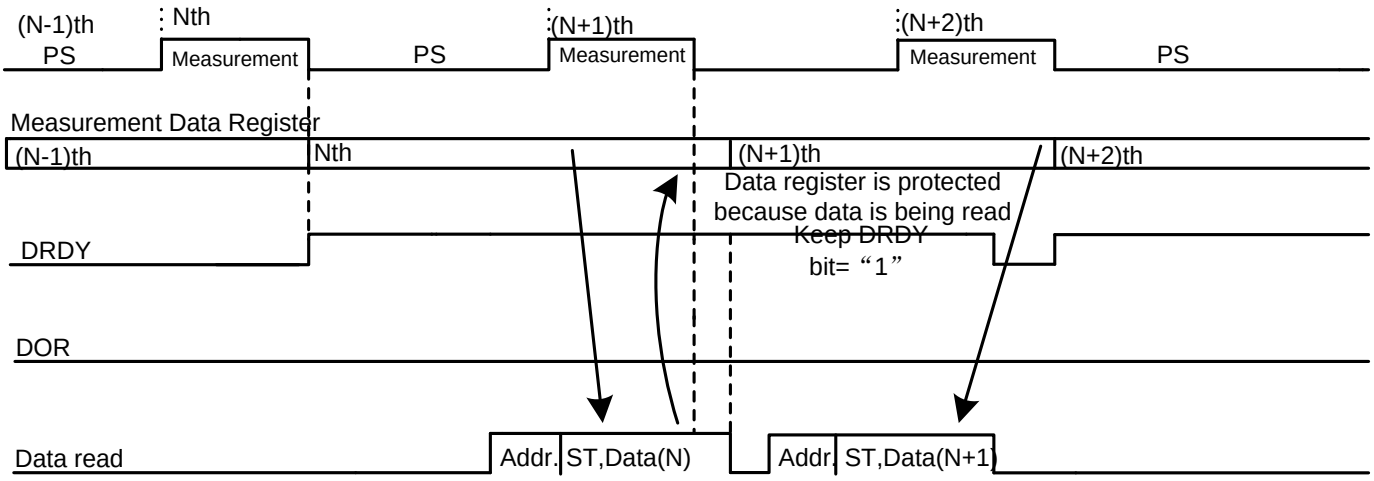


Figure 10.6 Data Not Skip: When data read has not been finished before the next measurement end

End Operation

Set Power-down mode (MODE[3:0] bits = “0000”) to end Continuous measurement mode.

Error Notification Function

Magnetic Sensor Overflow

OCH1970VAD-H has a limitation for measurement range, where the absolute value of X-axis and Y-axis should be smaller than 36.04 mT (High sensitivity mode) or 34.91 mT (Wide range mode). When the magnetic field exceeds this limitation, OCH1970VAD-H outputs limitation value at the X-axis or/and Y-axis (fixed value: 36.04 mT or 34.91 mT). This is called magnetic sensor overflow. When magnetic sensor overflow occurs, ERRXY bit turns to “1”. When the magnetic field less than limitation value, measurement data register (HX and HY) and ERRXY bit are updated.

ADC Overflow

OCH1970VAD-H has a limitation for ADC range, when the magnetic field exceeded this limitation, data stored at measurement data register (HX, HY and HZ) are not correct. This is called ADC overflow. When ADC overflow occurs, ERRADC bit turns to “1”.When measurement data registers are updated, ERRADC bit is updated.

Sensor Drive Select

Users can choose “Low power” or “Low noise” drive by the SDR bit.

“Low power” is used to save the current consumption and “Low noise” is used to reduce the noise of the OCH1970VAD-H. When Low noise (SDR bit = “0”) is set, output magnetic data noise is more reduced than Low power (about 50% of Low power). When Low power (SDR bit = “1”) is set, average current consumption at 10 Hz repetition rate is saved from 24 μA to 14 μA (VDD=1.8V, +25˚C). Default SDR bit is Low noise enable (SDR bit = “0”).

Sensor Measurement Range and Sensitivity Select

Users can choose “High sensitivity (Normal measurement range and high sensitivity)” or “Wide range (Wide measurement range and normal sensitivity)” setting.

“High sensitivity” is used to measure with high magnetic sensitivity and “Wide range” is used to measure strong magnetic field. When High sensitivity (SMR bit = “0”) is set, magnetic sensor sensitivity is about three times higher than Wide range (3.1 μT/LSB →1.1μT/LSB). When Wide range (SMR bit = “1”) is set, Z-axis measurement range is about three times wider than High sensitivity (Z-axis measurement range:±36.04 mT→ ±101.57 mT). Default SMR bit is High sensitivity enable (SMR bit =“0”).

Serial Interface

OCH1970VAD-H supports I2C bus interface and 4-wire SPI. A selection is made by CSB pin. When used as 3-wire SPI, set SI pin and SO pin wired-OR externally.
CSB pin = "L": 4-wire SPI
CSB pin = "H": I2C bus interface

■ 4-wire SPI

The 4-wire SPI consists of four digital signal lines: SK, SI, SO, and CSB, and is provided in 16bit protocol. Data consists of Read/Write control bit (R/W), register address (7-bit) and control data (8-bit). To read out all axis measurement data (X, Y, Z), an option to read out more than one byte data using automatic increment command is available. (Sequential read operation)

CSB pin is low active. Input data is taken in on the rising edge of SK pin, and output data is changed on the falling edge of SK pin. (SPI-mode3)
Communication starts when CSB pin transits to "L" and stops when CSB pin transits to "H". SK pin must be "H" during CSB pin is in transition. Also, it is prohibited to change SI pin during CSB pin is "H" and SK pin is "H

Writing Data

Input 16 bits data on SI pin in synchronous with the 16-bit serial clock input on SK pin. Out of 16 bits input data, the first 8-bit specify the R/W control bit (R/W = "0" when writing) and register address (7-bit), and the latter 8-bit are control data (8-bit). When any of addresses listed on Table 12.2 is input, OCH1970VAD-H recognizes that it is selected and takes in latter 8-bit as setting data.
If the number of clock pulses is less than 16, no data is written. It is compliant with serial write operation for multiple addresses. OCH1970VAD-H has one increment line; 20h to 27h. OCH1970VAD-H increments as follows: 20h→21h →22h →23h ... →27h →20h →21h ……

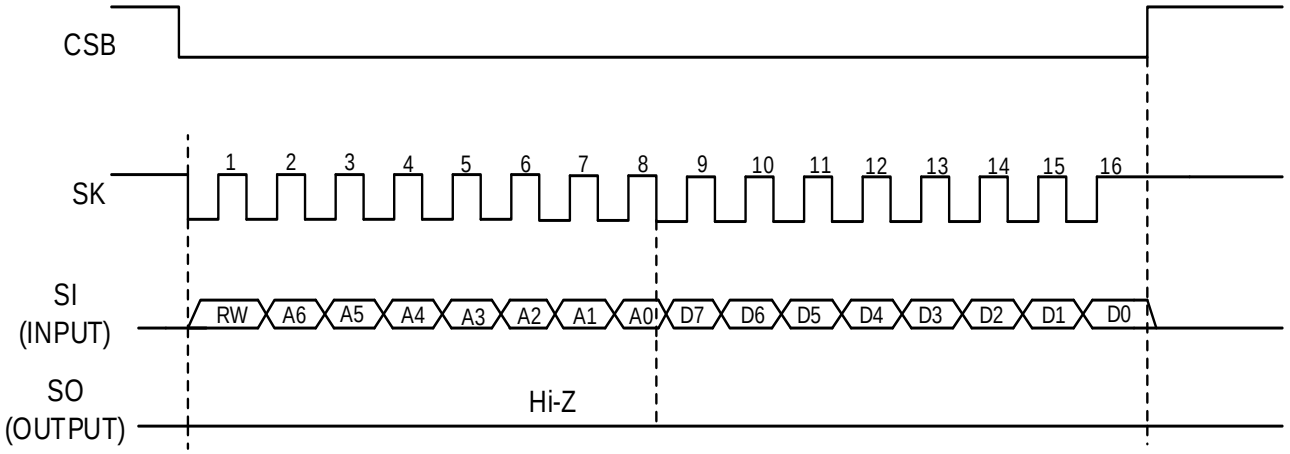


Figure 11.1 4-wire SPI writing data

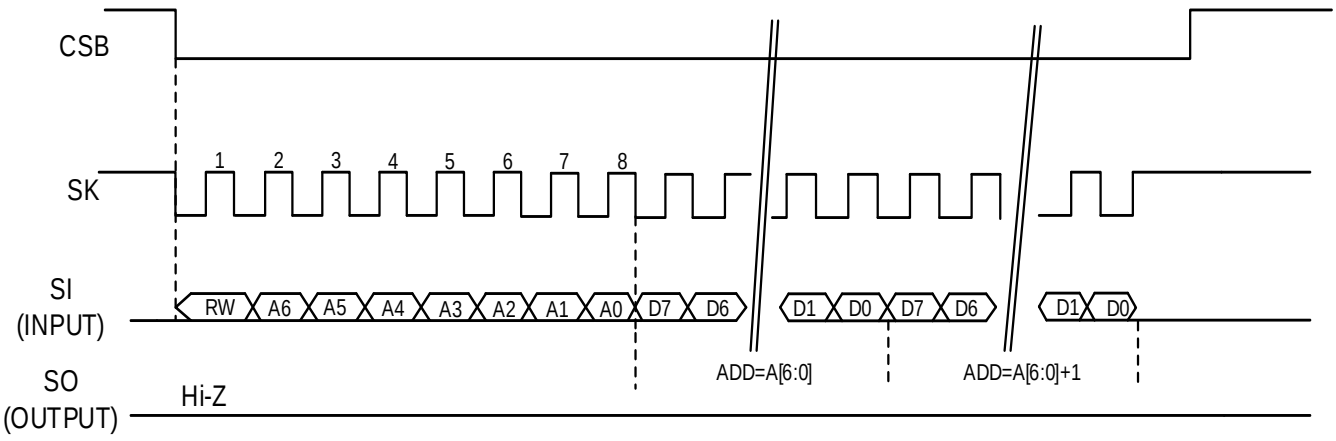


Figure 11.2 4-wire SPI serial writing data

Reading Data

Input the R/W control bit (R/W = “1”) and 7-bit register address on SI pin in synchronous with the first 8-bit of the 16 bits of a serial clock input on SK pin. Then OCH1970VAD-H outputs the data held in the specified register with MSB first from SO pin.

When clocks are input continuously after one byte of data is read, the address is incremented and data in the next address is output. Accordingly, after the falling edge of the 15th clock and CSB pin is “L”, the data in the next address is output on SO pin. When CSB pin is driven “L” to “H”, SO pin is placed in the high-impedance state. OCH1970VAD-H has one increment line; 20h to 27h. OCH1970VAD-H increments as follows: 20h ⓪ 21h ⓪ 22h ⓪23h ... ⓪ 27h ⓪ 20h ⓪ 21h.

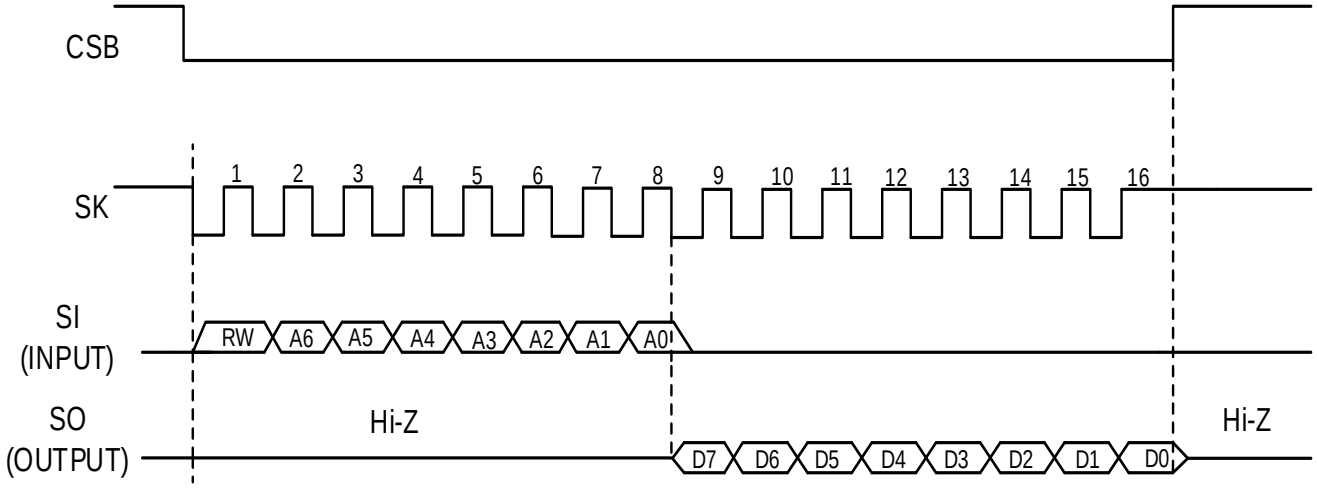


Figure 11.3 4-wire SPI reading data

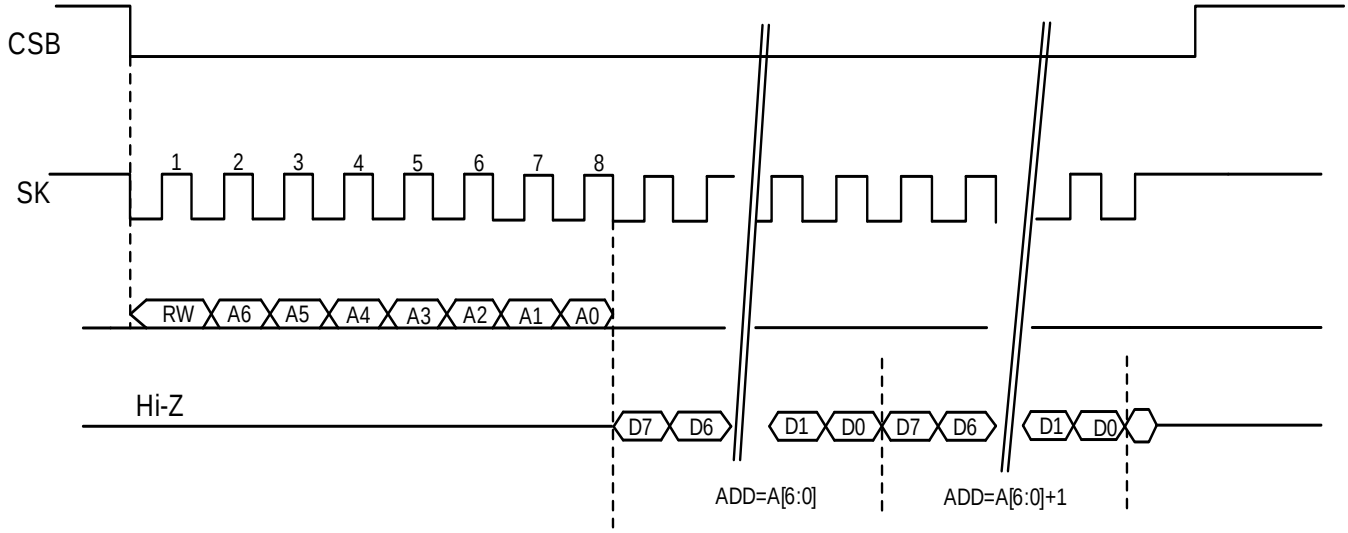


Figure 11.4 4-wire SPI serial reading data

■ I²C Bus Interface

The I2C bus interface of OCH1970VAD-H supports the Standard mode (100 kHz max.) and the Fast mode (400 kHz max.).

Data Transfer

To access OCH1970VAD-H on the bus, generate a start condition first.
Next, transmit a one-byte slave address including a device address. At this time, OCH1970VAD-H compares the slave address with its own address. If these addresses match, OCH1970VAD-H generates an acknowledgement, and then executes READ or WRITE instruction. At the end of instruction execution, generate a stop condition.

Change of Data

A change of data on the SDA line must be made during “Low” period of the clock on the SCL line. When the clock signal on the SCL line is “High”, the state of the SDA line must be stable. (Data on the SDA line can be changed only when the clock signal on the SCL line is “Low”.)
During the SCL line is “High”, the state of data on the SDA line is changed only when a start condition or a stop condition is generated.

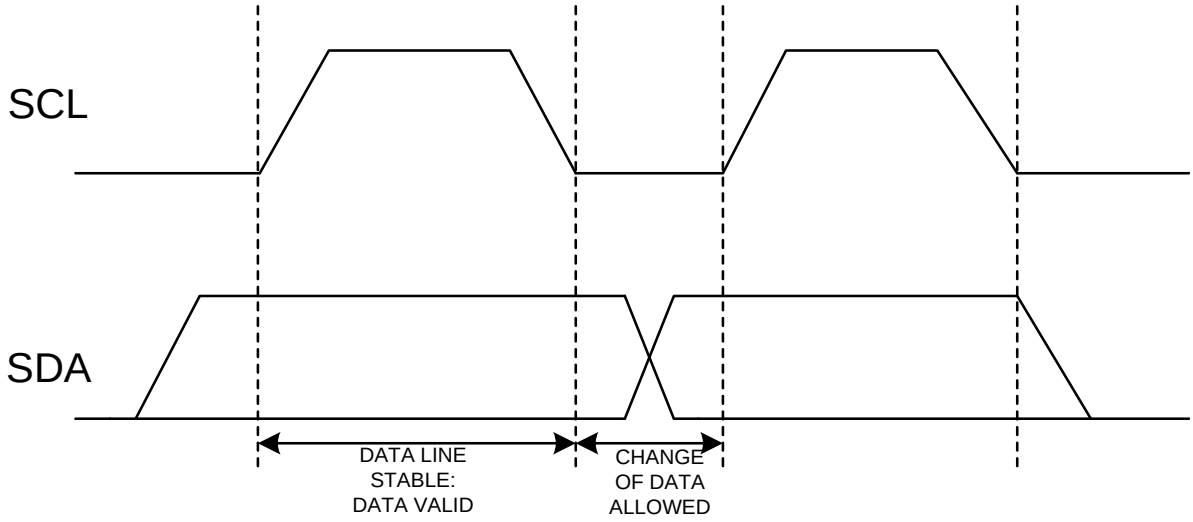


Figure 11.5 Data Change

Start/Stop Condition

If the SDA line is driven to “Low” from “High” when the SCL line is “High”, a start condition is generated. Every instruction starts with a start condition.
If the SDA line is driven to “High” from “Low” when the SCL line is “High”, a stop condition is generated. Every instruction stops with a stop condition.

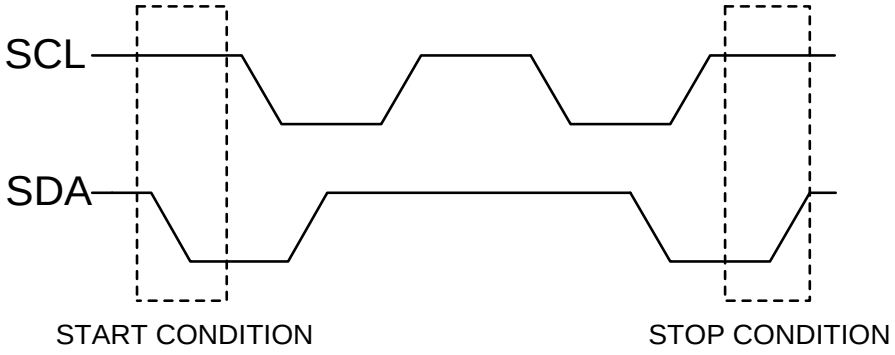


Figure 11.6 Start and stop condition

Acknowledge

The IC that is transmitting data releases the SDA line (in the “High” state) after sending 1-byte data. The IC that receives the data drives the SDA line to “Low” on the next clock pulse. This operation is referred as an acknowledge. With this operation, whether data has been transferred successfully can be checked. OCH1970VAD-H generates an acknowledge after receipt of the start condition and slave address.

When a WRITE instruction is executed, OCH1970VAD-H generates an acknowledge after every byte that is received. When a READ instruction is executed, OCH1970VAD-H generates an acknowledge then transfers the data stored at the specified address. Next, OCH1970VAD-H releases the SDA line then monitors the SDA line. If a master IC generates an acknowledge instead of a stop condition, OCH1970VAD-H transmits the 8-bit data stored at the next address. If no acknowledge is generated, OCH1970VAD-H stops data transmission.

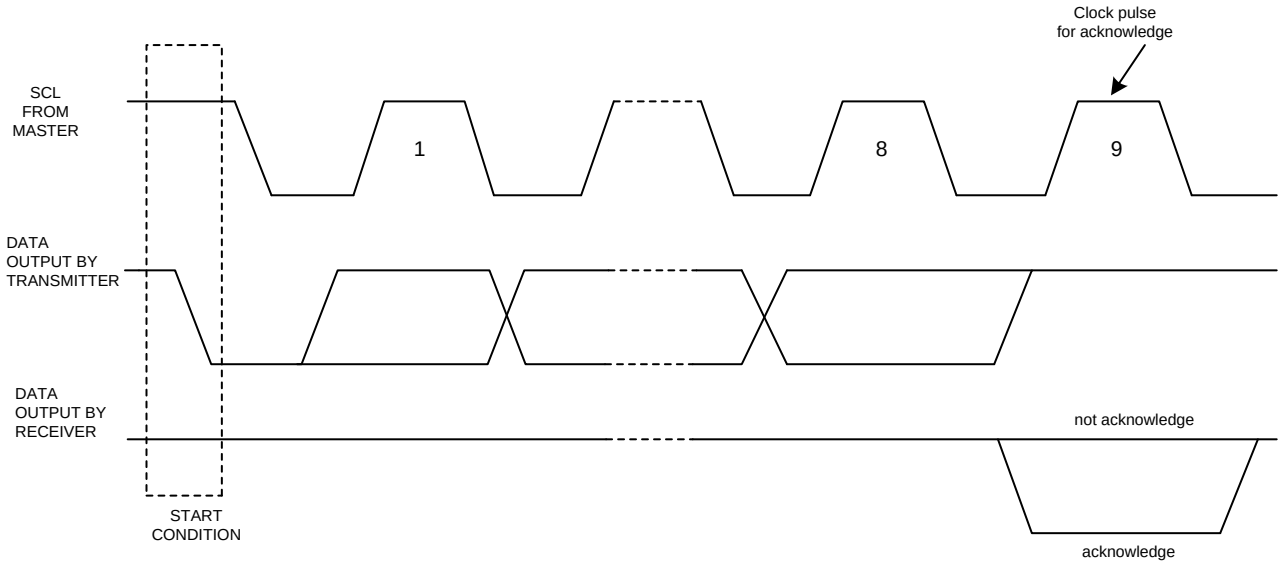


Figure 11.7 Generation of acknowledge

Slave Address

The slave address of OCH1970VAD-H can be selected from the following list by setting CAD0/1 pin. When CAD pin is fixed to VSS, the corresponding slave address bit is “0“. When CAD pin is fixed to VDD, the corresponding slave address bit is “1”.

Table 11.1 Slave address and CAD pin

CAD	Slave Address
0	0Ch
1	0Dh

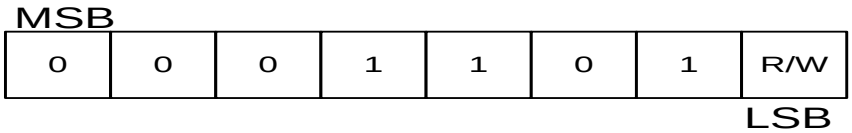


Figure 11.8 Slave address

The first byte including a slave address is transmitted after a start condition, and an IC to be accessed is selected from the ICs on the bus according to the slave address.

When a slave address is transferred, the IC whose device address matches the transferred slave address generates an acknowledge then executes an instruction. The 8th bit (least significant bit) of the first byte is a R/W bit. When the R/W bit is set to “1“, READ instruction is executed. When the R/W bit is set to “0“, WRITE instruction is executed.

WRITE Instruction

When the R/W bit is set to “0”, OCH1970VAD-H performs write operation.

In write operation, OCH1970VAD-H generates an acknowledge after receiving a start condition and the first byte (slave address) then receives the second byte. The second byte is used to specify the address of an internal control register and is based on the MSB-first configuration.

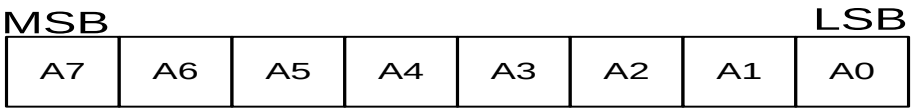


Figure 11.9 Register address

After receiving the second byte (register address), OCH1970VAD-H generates an acknowledge then receives the third byte.

The third and the following bytes represent control data. Control data consists of 8-bit and is based on the MSB-first configuration. OCH1970VAD-H generates an acknowledge after every byte is received. Data transfer always stops with a stop condition generated by the master.

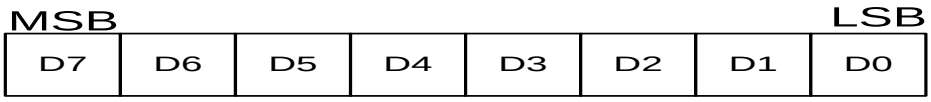


Figure 11.10 Control data

OCH1970VAD-H can write multiple bytes of data at a time.

After reception of the third byte (control data), OCH1970VAD-H generates an acknowledge then receives the next data. If additional data is received instead of a stop condition after receiving one byte of data, the address counter inside the LSI chip is automatically incremented and the data is written at the next address.

The address is incremented from 20h to 27h. When the address is between 20h and 27h, the address is incremented 20h →21h →22h →23h…27h,and the address goes back to 20h after 27h.

Actual data is written only to Read/Write registers.

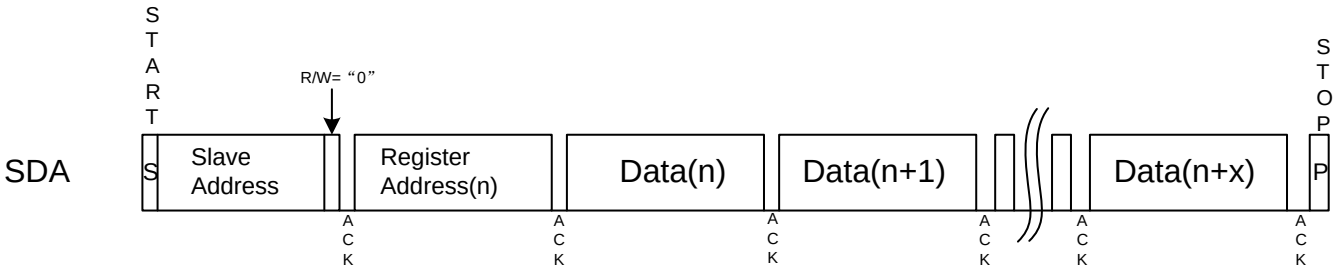


Figure 11.11 WRITE Instruction

READ Instruction

When the R/W bit is set to "1", OCH1970VAD-H performs read operation.

If a master IC generates an acknowledge instead of a stop condition after OCH1970VAD-H transfers the data at a specified address, the data at the next address can be read.

Address can be 20h to 27h. When the address is between 20h and 27h, the address is incremented 20h → 21h → 22h → 23h ... →27h, and the address goes back to 20h after 27h. OCH1970VAD-H supports one byte read and multiple byte read.

Current Address Read

OCH1970VAD-H has an address counter inside the LSI chip. In current address read operation, the data at an address specified by this counter is read.

The internal address counter holds the next address of the most recently accessed address.

For example, if the address most recently accessed (for READ instruction) is address "n", and a current address read operation is attempted, the data at address "n+1" is read.

In current address read operation, OCH1970VAD-H generates an acknowledge after receiving a slave address for the READ instruction (R/W bit = "1"). Next, OCH1970VAD-H transfers the data specified by the internal address counter starting with the next clock pulse, then increments the internal counter by one. If the master IC generates a stop condition instead of an acknowledge after OCH1970VAD-H transmits one byte of data, the read operation stops.

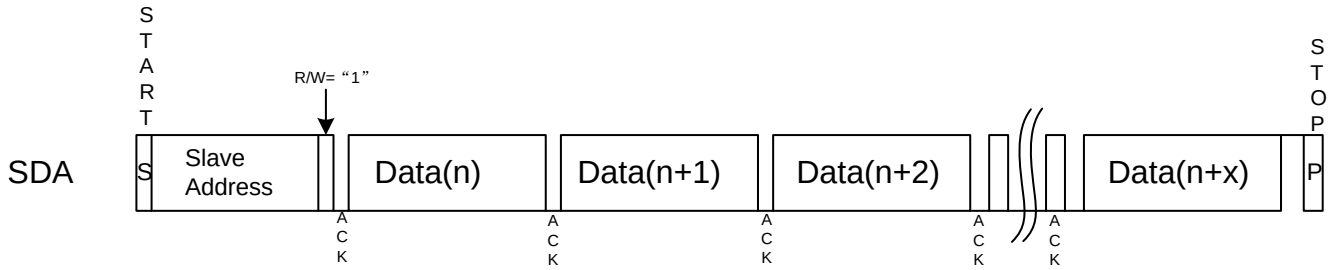


Figure 11.12 Current address read

Random Address Read

By random address read operation, data at an arbitrary address can be read.

The random address read operation requires to execute WRITE instruction as dummy before a slave address for the READ instruction (R/W bit = “1”) is transmitted. In random read operation, a start condition is first generated then a slave address for the WRITE instruction (R/W bit = “0”) and a read address are transmitted sequentially.

After OCH1970VAD-H generates an acknowledge in response to this address transmission, a start condition and a slave address for the READ instruction (R/W bit = “1”) are generated again. OCH1970VAD-H generates an acknowledge in response to this slave address transmission. Next, OCH1970VAD-H transfers the data at the specified address then increments the internal address counter by one. If the master IC generates a stop condition instead of an acknowledge after data is transferred, the read operation stops.

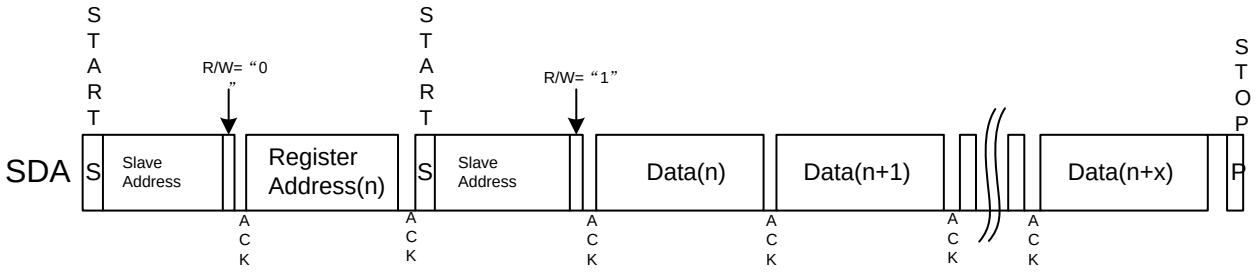


Figure 11.13 Random address read

■ Registers

Description of Registers

OCH1970VAD-H has registers of 29 addresses as indicated in Table 12.1. Every address consists of 1-byte to 8-byte data. Data is transferred to or received from the external CPU via the serial interface described previously.

Table 12.1 Register Table

Address	READ/ WRIT	Description	Byte widt	Remarks
00H	READ	Company ID, Device ID	4	Device Information
10H		Status	2	ST data
11H		Status and Measurement Magnetic Data	4	ST + X-axis data
12H			4	ST + Y-axis data
13H			6	ST + X and Y-axis data
14H			4	ST + Z-axis data
15H			6	ST + X and Z-axis data
16H			6	ST + Y and Z-axis data
17H			8	ST + X,Y and Z-axis data
18H		Status and Measurement Magnetic Data (upper 8 bits of measurement data register)	2	ST data
19H			3	ST + X-axis data
1AH			3	ST + Y-axis data
1BH			4	ST + X and Y-axis data
1CH			3	ST + Z-axis data
1DH			4	ST + X and Z-axis data
1EH			4	ST + Y and Z-axis data
1FH			5	ST + X,Y and Z-axis data
21H		Control 2	1	Operation Mode, Sensor Drive, Measurement Range and Sensitivity
30H		Reset	1	Soft reset
31H		I2C disable	1	
40H		Test	2	DO NOT ACCESS
41H			1	DO NTO ACCESS

Addresses 20h to 27h are compliant with automatic increment function of serial interface respectively. When the address is in 20h to 27h, the address is incremented 20h→ 21h → 22h → 23h ... →27h, and the address goes back to 20h after 27h.

Register Map

Table 12.2 Register Map

Addr.	Byte0	Byte1	Byte2	Byte3	Byte4	Byte5	Byte6	Byte7
Read only register								
00H	WIA[15:8]	WIA[7:0]	RSV[15:8]	RSV[7:0]	-	-	-	-
10H	ST[15:8]	ST[7:0]	-	-	-	-	-	-
11H	ST[15:8]	ST[7:0]	HX[15:8]	HX[7:0]	-	-	-	-
12H	ST[15:8]	ST[7:0]	HY[15:8]	HY[7:0]	-	-	-	-
13H	ST[15:8]	ST[7:0]	HY[15:8]	HY[7:0]	HX[15:8]	HX[7:0]	-	-
14H	ST[15:8]	ST[7:0]	HZ[15:8]	HZ[7:0]	-	-	-	-
15H	ST[15:8]	ST[7:0]	HZ[15:8]	HZ[7:0]	HX[15:8]	HX[7:0]	-	-
16H	ST[15:8]	ST[7:0]	HZ[15:8]	HZ[7:0]	HY[15:8]	HY[7:0]	-	-
17H	ST[15:8]	ST[7:0]	HZ[15:8]	HZ[7:0]	HY[15:8]	HY[7:0]	HX[15:8]	HX[7:0]
18H	ST[15:8]	ST[7:0]	-	-	-	-	-	-
19H	ST[15:8]	ST[7:0]	HX[15:8]	-	-	-	-	-
1AH	ST[15:8]	ST[7:0]	HY[15:8]	-	-	-	-	-
1BH	ST[15:8]	ST[7:0]	HY[15:8]	HX[15:8]	-	-	-	-
1CH	ST[15:8]	ST[7:0]	HZ[15:8]	-	-	-	-	-
1DH	ST[15:8]	ST[7:0]	HZ[15:8]	HX[15:8]	-	-	-	-
1EH	ST[15:8]	ST[7:0]	HZ[15:8]	HY[15:8]	-	-	-	-
1FH	ST[15:8]	ST[7:0]	HZ[15:8]	HY[15:8]	HX[15:8]	-	-	--
Read/Write register								
20H	CNTL1[15:8]	CNTL1[7:8]	-	-	-	-	-	-
21H	CNTL2[7:0]	-	-	-	-	-	-	-
22H	RSV[15:8]	RSV[7:0]	RSV[15:8]	RSV[7:0]	-	-	-	-
23H	RSV[15:8]	RSV[7:0]	RSV[15:8]	RSV[7:0]	-	-	-	-
24H	RSV[15:8]	RSV[7:0]	RSV[15:8]	RSV[7:0]	-	-	-	-
25H	RSV[15:8]	RSV[7:0]	RSV[15:8]	RSV[7:0]	-	-	-	-
26H	RSV[15:8]	RSV[7:0]	RSV[15:8]	RSV[7:0]	-	-	-	-
27H	RSV[15:8]	RSV[7:0]	RSV[15:8]	RSV[7:0]	-	-	-	-
30H	SRST[7:0]	-	-	-	-	-	-	-
31H	I2CDIS[7:0]	-	-	-	-	-	-	-
40H								
41H								

Table 12.3 Further details about Register Map (D[7:0])

Register name	Bit number (D[7:0])							
	7	6	5	4	3	2	1	0
WIA[7:0]	1	1	0	0	0	0	0	0
RSV[7:0]	RSV7	RSV6	RSV5	RSV4	RSV3	RSV2	RSV1	RSV0
ST[7:0]	ERRXY	RSV6	RSV5	RSV4	RSV3	RSV2	RSV1	DRDY
RSV[7:0]	HX7	HX6	HX5	HX4	HX3	HX2	HX1	HX0
RSV[7:0]	HY7	HY6	HY5	HY4	HY3	HY2	HY1	HY0
HZ[7:0]	HZ7	HZ6	HZ5	HZ4	HZ3	HZ2	HZ1	HZ0
CNTL1[7:0]	ERRXYEN	RSV6	RSV5	RSV4	RSV3	RSV2	RSV1	DRDYEN
CNTL2[7:0]	0	0	SMR	SDR	MODE3	MODE2	MODE1	MODE0
RSV[7:0]	RSV7	RSV6	RSV5	RSV4	RSV3	RSV2	RSV1	RSV0
RSV[7:0]	RSV7	RSV6	RSV5	RSV4	RSV3	RSV2	RSV1	RSV0
RSV[7:0]	RSV7	RSV6	RSV5	RSV4	RSV3	RSV2	RSV1	RSV0
RSV[7:0]	RSV7	RSV6	RSV5	RSV4	RSV3	RSV2	RSV1	RSV0
RSV[7:0]	RSV7	RSV6	RSV5	RSV4	RSV3	RSV2	RSV1	RSV0
RSV[7:0]	RSV7	RSV6	RSV5	RSV4	RSV3	RSV2	RSV1	RSV0
RSV[7:0]	RSV7	RSV6	RSV5	RSV4	RSV3	RSV2	RSV1	RSV0
RSV[7:0]	RSV7	RSV6	RSV5	RSV4	RSV3	RSV2	RSV1	RSV0
RSV[7:0]	RSV7	RSV6	RSV5	RSV4	RSV3	RSV2	RSV1	RSV0
RSV[7:0]	RSV7	RSV6	RSV5	RSV4	RSV3	RSV2	RSV1	RSV0
RSV[7:0]	RSV7	RSV6	RSV5	RSV4	RSV3	RSV2	RSV1	RSV0
RSV[7:0]	RSV7	RSV6	RSV5	RSV4	RSV3	RSV2	RSV1	RSV0
SRST[7:0]	0	0	0	0	0	0	0	SRST
I2CDIS[7:0]	I2CDIS7	I2CDIS6	I2CDIS5	I2CDIS4	I2CDIS3	I2CDIS2	I2CDIS1	I2CDIS0
TEST1[7:0]	-	-	-	-	-	-	-	-
TEST2[7:0]								

Table 12.4 Further details about Register Map (D[15:8])

Register name	Bit number (D[15:8])							
	15	14	13	12	11	10	9	8
WIA[15:8]	0	1	0	0	1	0	0	0
RSV[15:8]	RSV15	RSV14	RSV13	RSV12	RSV11	RSV10	RSV9	RSV8
ST[15:8]	1	1	1	1	1	1	DOR	ERRADC
RSV[15:8]	HX15	HX14	HX13	HX12	HX11	HX10	HX9	HX8
RSV[15:8]	HY15	HY14	HY13	HY12	HY11	HY10	HY9	HY8
HZ[15:8]	HZ15	HZ14	HZ13	HZ12	HZ11	HZ10	HZ9	HZ8
CNTL1[15:8]	0	0	0	0	0	RSV10	RSV9	ERRADCEN
CNTL2[15:8]	-	-	-	-	-	-	-	-
RSV[15:8]	RSV15	RSV14	RSV13	RSV12	RSV11	RSV10	RSV9	RSV8
RSV[15:8]	RSV15	RSV14	RSV13	RSV12	RSV11	RSV10	RSV9	RSV8
RSV[15:8]	RSV15	RSV14	RSV13	RSV12	RSV11	RSV10	RSV9	RSV8
RSV[15:8]	RSV15	RSV14	RSV13	RSV12	RSV11	RSV10	RSV9	RSV8
RSV[15:8]	RSV15	RSV14	RSV13	RSV12	RSV11	RSV10	RSV9	RSV8
RSV[15:8]	RSV15	RSV14	RSV13	RSV12	RSV11	RSV10	RSV9	RSV8
RSV[15:8]	RSV15	RSV14	RSV13	RSV12	RSV11	RSV10	RSV9	RSV8
RSV[15:8]	RSV15	RSV14	RSV13	RSV12	RSV11	RSV10	RSV9	RSV8
RSV[15:8]	RSV15	RSV14	RSV13	RSV12	RSV11	RSV10	RSV9	RSV8
RSV[15:8]	RSV15	RSV14	RSV13	RSV12	RSV11	RSV10	RSV9	RSV8
RSV[15:8]	RSV15	RSV14	RSV13	RSV12	RSV11	RSV10	RSV9	RSV8
RSV[15:8]	RSV15	RSV14	RSV13	RSV12	RSV11	RSV10	RSV9	RSV8
SRST[15:8]	-	-	-	-	-	-	-	-
I2CDIS[15:8]	I2CDIS15	I2CDIS14	I2CDIS13	I2CDIS12	I2CDIS11	I2CDIS10	I2CDIS9	I2CDIS8
TEST1[15:8]	-	-	-	-	-	-	-	-
TEST2[15:8								

When RSTN pin is applied VDD, all registers of OCH1970VAD-H are initialized.
TEST1 and TEST2 is test register for shipment test. Do not access this register.

Detailed Description of Registers
WIA[15:0] Company ID and Device ID

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read-only register									
00h	WIA[7:0]	1	1	0	0	0	0	0	0
Addr.	**Register name**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Read-only register									
00h	WIA[15:8]	0	1	0	0	1	0	0	0

WIA[7:0] bits: Device ID of OCS. It is described in one byte and fixed value. C0h: fixed
WIA[15:8] bits: Company ID of OCH1970VAD-H. It is described in one byte and fixed value. 48h: fixed

RSV[15:0]:ReservedRegister

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read-only register									
00h	RSV[7:0]	RSV7	RSV6	RSV5	RSV4	RSV3	RSV2	RSV1	RSV0
Addr.	**Register name**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Read-only register									
00h	RSV[15:8]	RSV15	RSV14	RSV13	RSV12	RSV11	RSV10	RSV9	RSV8

RSV[7:0] bits/ RSV[15:8] bits: Reserved register for OCS.

ST[15:0]:Status

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read-only register									
10h-1fh	ST[7:0]	ERRXY	RSV6	RSV5	RSV4	RSV3	RSV2	RSV1	DRDY
Reset		0	0	0	0	0	0	0	0
Addr.	**Register name**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Read-only register									
10h-1fh	ST[15:8]	1	1	1	1	1	1	DOR	ERRADC
Reset		1	1	1	1	1	1	0	0

DRDY bit: Data Ready

“0”: Normal
“1”: Data is ready

DRDY bit turns to “1” when data is ready in Single measurement mode and Continuous measurement mode 1, 2, 3, 4, 5, 6, and 7. It returns to “0” when Z-axis measurement data register is read all the way through or access to Setting Registers (address 20h to 27h).

DOR bit: Data Overrun
“0”: Normal
“1”: Data overrun

DOR bit turns to “1” when data has been skipped in Continuous measurement mode 1, 2, 3, 4, 5, 6 or 7.
DOR bit turns to “0” at the after the next measurement ended.

ERRXY bit: Magnetic sensor overflow
“0”: Normal
“1”: Magnetic sensor overflow occurred (X and/or Y-axis)

ERRADC bit: ADC overflow
“0”: Normal
“1”: ADC overflow occurred and measurement data is not correct

HZ[15:0]:Measurement Data

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read-only register									
10h	HX[7:0]	HX7	HX6	HX5	HX4	HX3	HX2	HX1	HX0
|	HY[7:0]	HY7	HY6	HY5	HY4	HY3	HY2	HY1	HY0
1f	HZ[7:0]	HZ7	HZ6	HZ5	HZ4	HZ3	HZ2	HZ1	HZ0
Reset		0	0	0	0	0	0	0	0
Addr.	**Register name**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Read-only register									
10h	HX[15:8]	HX15	HX14	HX13	HX12	HX11	HX10	HX9	HX8
|	HY[15:8]	HY15	HY14	HY13	HY12	HY11	HY10	HY9	HY8
1f	HZ[15:8]	HZ15	HZ14	HZ13	HZ12	HZ11	HZ10	HZ9	HZ8
Reset		0	0	0	0	0	0	0	0

Measurement data of magnetic sensor X-axis/Y-axis/Z-axis
HX[7:0] bits: X-axis measurement data lower 8-bit
HX[15:8] bits: X-axis measurement data higher 8-bit
HY[7:0] bits: Y-axis measurement data lower 8-bit
HY[15:8] bits: Y-axis measurement data higher 8-bit
HZ[7:0] bits: Z-axis measurement data lower 8-bit
HZ[15:8] bits: Z-axis measurement data higher 8-bit
Measurement data is stored in two’s complement. Measurement range of each axis is -32768 to 32767 in 16-bit output (High sensitivity setting). Measurement range of X and Y-axis are -11264 to 11264 in 16-bit output, Z-axis is -32768 to 32767 in 16-bit output (Wide range setting).

Table 12.5 Measurement magnetic data format (High sensitivity setting)

Measurement data (each axis) [15:0] bits			Magnetic flux density [mT]	ERRXY bit
Two’s complement	Hex	Decimal		
0111 1111 1111 1111	7FFF	32767	>36.0437	1
0111 1111 1111 1111	7FFF	32767	36.0437	0
|	|	|	|	|
0000 0000 0000 0001	0001	1	0.0011	0
0000 0000 0000 0000	0000	0	0	0
1111 1111 1111 1111	FFFF	-1	-0.0011	0
|	|	|	|	|
1000 0000 0000 0000	8000	-32768	-36.0448	0
1000 0000 0000 0000	8000	-32768	<-36.0448	1

Table 12.6 Measurement magnetic data format (Wide range setting, X and Y-axis)

Measurement data (X and Y axis) [15:0] bits			Magnetic flux density [mT]	ERRXY bit
Two's complement	Hex	Decimal		
0010 1100 0000 0000	2C00	11264	>34.9184	1
0010 1100 0000 0000	2C00	11264	34.9184	0
|	|	|	|	|
0000 0000 0000 0001	0001	1	0.0031	0
0000 0000 0000 0000	0000	0	0	0
1111 1111 1111 1111	FFFF	-1	-0.0031	0
|	|	|	|	|
1101 0100 0000 0000	D400	-11264	-34.9184	0
1101 0100 0000 0000	D400	-11264	<-34.9184	1

Table 12.7 Measurement magnetic data format (Wide range setting, Z-axis)

Measurement data (Z axis) [15:0] bits			Magnetic flux density [mT]
Two's complement	Hex	Decimal	
0111 1111 1111 1111	7FFF	32767	>101.5777
0111 1111 1111 1110	7FFE	32766	101.5746
|	|	|	|
0000 0000 0000 0001	0001	1	0.0031
0000 0000 0000 0000	0000	0	0
1111 1111 1111 1111	FFFF	-1	-0.0031
|	|	|	|
1000 0000 0000 0001	8001	-32767	-101.5777
1000 0000 0000 0000	8000	-32768	<-101.5808

CNTL1[15:0]:Interrupt Output Setting

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read/Write register									
20h	CNTL1[7:0]	ERRXYEN	RSV6	RSV5	RSV4	RSV3	RSV2	RSV1	DRDYEN
Reset		0	0	0	0	0	0	0	1
Addr.	**Register name**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Read/Write register									
20h	CNTL1[15:8]	0	0	0	0	0	RSV10	RSV9	ERRADCEN
Reset		0	0	0	0	0	1	1	0

DRDYEN bit: DRDY event output
"0": DRDY event outputs disable
"1": DRDY event outputs enable

ERRXYEN bit: ERRXY event output "0": ERRXY event outputs disable "1": ERRXY event outputs enable

ERRADCEN bit: ERRADC event output
"0": ERRADC event outputs disable
"1": ERRADC event outputs enable

CNTL2[7:0]:Operation Mode, Sensor Drive, Measurement Range and Sensitivity setting

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read/Write register									
21h	CNTL2[7:0]	0	0	SMR	SDR	MODE3	MODE2	MODE1	MODE0
Reset		0	0	0	0	0	0	0	0

MODE[3:0] bits: Operation mode setting
"0000": Power-down mode
"0001": Single measurement mode
"0010": Continuous measurement mode 1
"0100": Continuous measurement mode 2
"0110": Continuous measurement mode 3
"1000": Continuous measurement mode 4
"1010": Continuous measurement mode 5
"1100": Continuous measurement mode 6
"1110": Continuous measurement mode 7
SDR bit: Sensor drive setting
"0": Low noise drive
"1": Low power drive

SMR bit: Measurement range and sensitivity setting
"0": High sensitivity setting
"1": Wide measurement range setting

SRST[7:0]:Soft Reset

Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read/Write register									
11h	SRST[7:0]	0	0	0	0	0	0	0	SRST
Reset		0	0	0	0	0	0	0	0

SRST bit: Soft reset

"0": Normal
"1": Reset

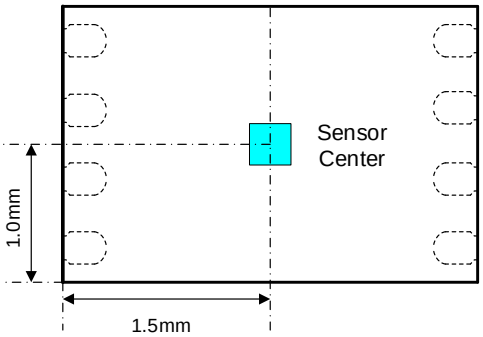
When "1" is set, all registers are initialized. After reset, SRST bit turns to "0" automatically.

Test register

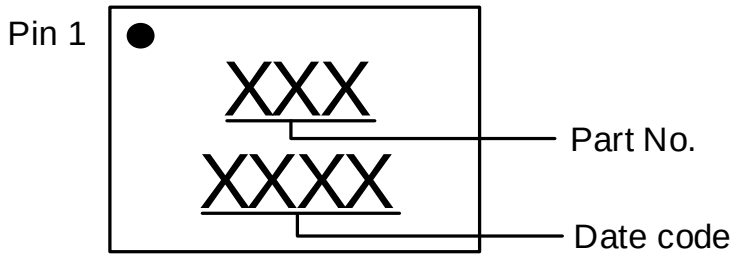
Addr.	Register name	D7	D6	D5	D4	D3	D2	D1	D0
Read/Write register									
40h	TST1	-	-	-	-	-	-	-	-
41h	TST2	-	-	-	-	-	-	-	-
Reset		0	0	0	0	0	0	0	0
Addr.	**Register name**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Read/Write register									
40h	TST1	-	-	-	-	-	-	-	-
41h	TST2	-	-	-	-	-	-	-	-
Reset		0	0	0	0	0	0	0	0

TST1 and TST2 register are test register for shipment test. Do not access this registers.

■ Hall Sensor Location

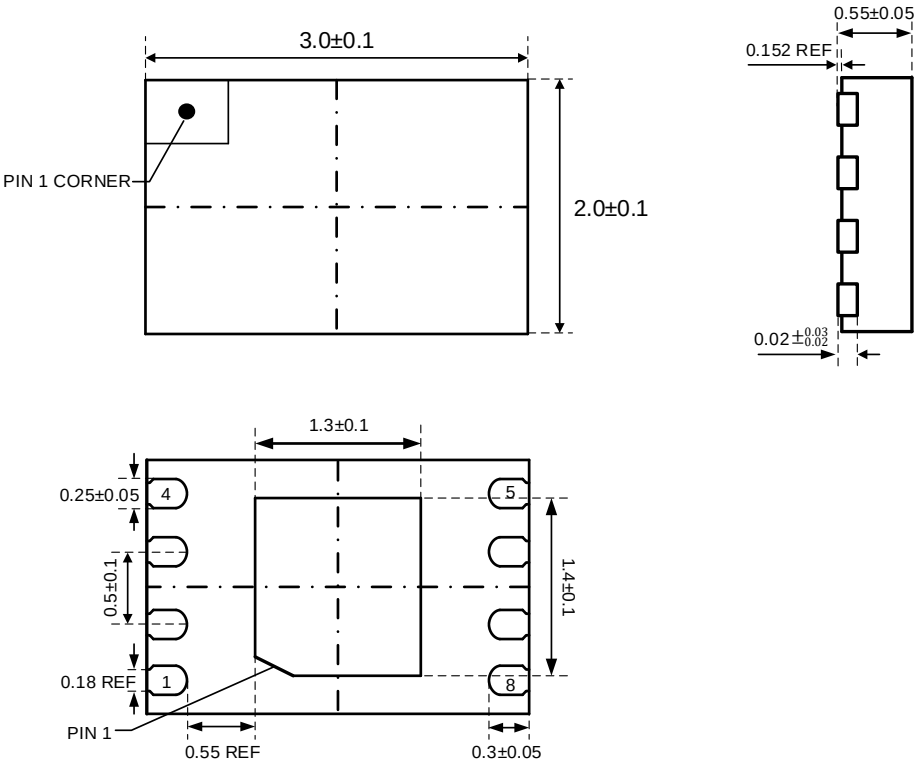


■ Marking Information



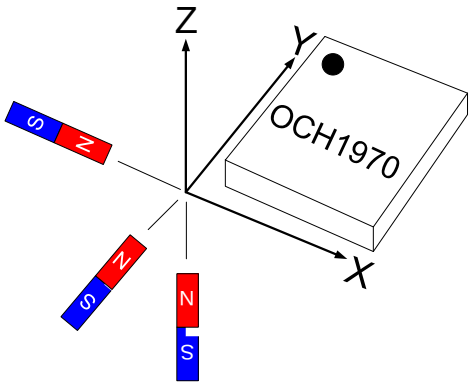
■ Package Information

1) DFN2030-8L



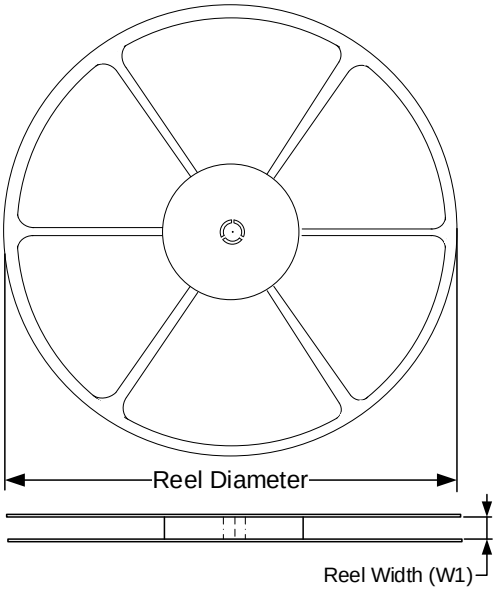
NOTE: All dimensions are in mm

■ Magnetic Orientation

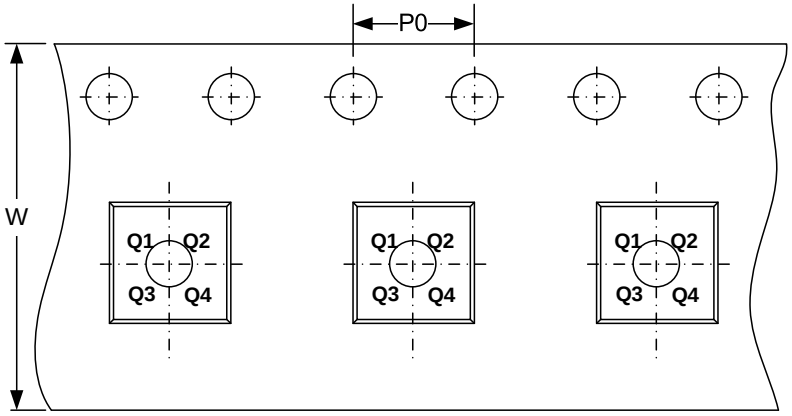


■ Packing Information

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

Package type	SPQ (PCS)	Reel Diameter (mm)	Reel Width W1(mm)	W (mm)	P0 (mm)	MSL	Pin 1 Quadrant
DFN2030-8L	3000	180	8.6	8.0	4.0	Level-3	Q2

Note: Carrier Tape Dimension, Reel Size and Packing Minimum.

IMPORTANT NOTICE

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