■ General Description

OCP1405 is a 500mA low dropout, low power linear regulator with NMOS pass transistor and a separate bias supply voltage. OCP1405 provides stable and accurate output for noise sensitive applications. OCP1405 also offers low current consumption for battery operated applications.

The device is a RoHS compliant DFN1212-6L package.

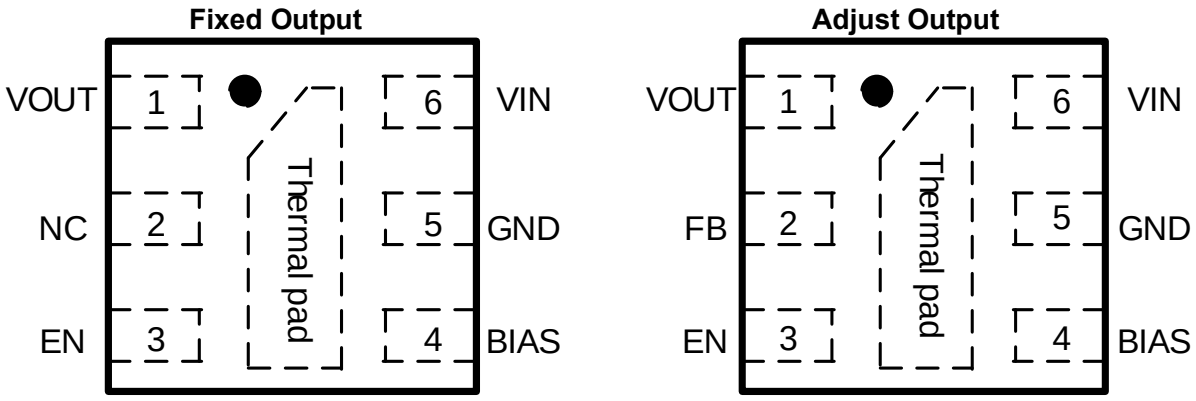
■ Applications

- Smartphones, Cellphone, PDAs
- Bluetooth, wireless handsets
- Portable equipment

■ Features

- Input Voltage Range: 0.8V to 5.5V
- Bias Voltage Range: 2.6V to 5.5V
- Output Voltage Ranger: 0.8V to 3.6V
- Output Current: 500mA
- Low Quiescent Current: 70μA(Typ)
- Shut Down Current: <1μA
- Dropout Voltage: 150mV @ 500mA
- PSRR-VIN: 70dB @ 1kHz
- PSRR-VBIAS：78dB @ 1KHz
- Auto-Discharge function
- Available in DFN1212-6L package
- -40°C to +85°C Operating Temperature Range

■ Pin Configuration



DFN1212-6L
(TOP View)

Figure 1, Pin Assignments of OCP1405

Pin Name	Pin Function		
	DFN1212-6L FIXED	DFN1212-6L ADJ	
VOUT	1	1	Regulator Output Pin. Bypass a 2.2μF capacitor to ground.
BIAS	4	4	Bias voltage supply for internal control circuits. This pin is monitored by internal Under-Voltage Lockout Circuit. Bypass a 0.1μF capacitor to ground.
EN	3	3	Enable control pin, active high. When EN pin is floating, it will be shutdown mode.
VIN	6	6	Regulator Input Pin. 1μF decouple capacitor is needed.
GND	5	5	Power Ground
FB	-	2	Feedback
NC	2	-	No Connection
Thermal pad	-	-	Thermal pad

Typical Application Circuit

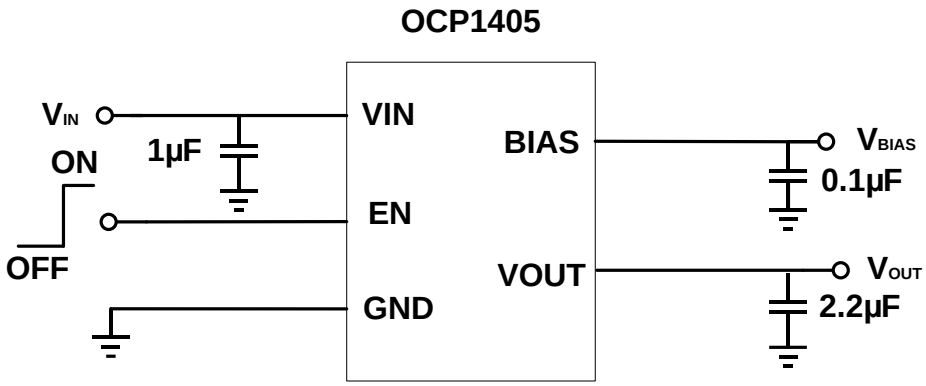


Figure 2, Fixed Voltage Typical Application Circuit of OCP1405

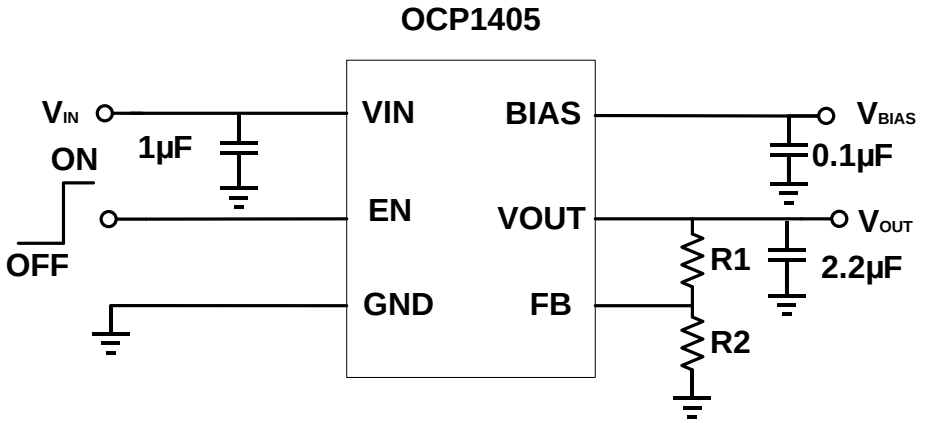


Figure 3, Adjustable Voltage Typical Application Circuit of OCP1405

■ Block Diagram

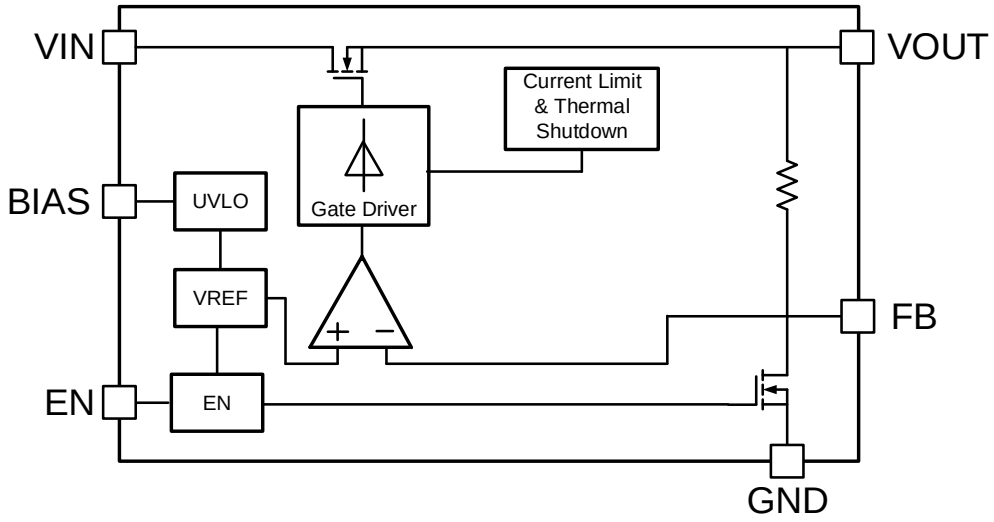


Figure 4. Adjustable Version Block Diagram

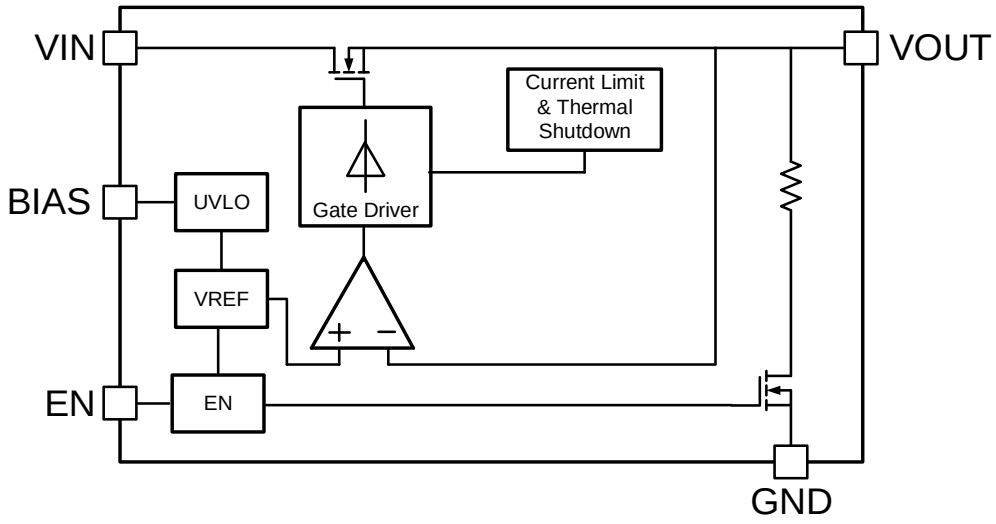


Figure 5. Fixed Version Block Diagram

■ Absolute Maximum Ratings[1] (T_A=25°C unless otherwise noted)

Parameter	Symbol	Rating	Unit
Input Voltage Range	V_{IN}	-0.3 to 6.5	V
Output Voltage Range	VOUT	-0.3 to 6.5	V
Enable Input And Bias Voltage Range	V_{EN}	-0.3 to 6.5	V
Maximum Load Current	I_{OUT}	600	mA
Human Body Model	HBM	5	kV
Charged Device Model	CDM	0.5	kV
Storage Temperature Range	T_S	-55 to +150	°C

Notes: 1)Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

■ Recommended Operating Conditions[2](T_A=25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Bias Input Voltage	V_{BIAS}	2.6 ~ 5.5	V
Ambient Operating Temperature	TA	-40 to 85	°C
Operating Junction Temperature Range	T_J	-40 to 125	°C
DFN1212-6，Thermal Resistance ,$R_{\theta JA}$	θ_{JA}	150	°C /W

Notes: 2) The device is not guaranteed to function outside of its operating conditions

■ Electrical Characteristics

(Unless otherwise noted, test values are at T_A=25°C, V_{IN}= VOUT + 0.3V, V_{BIAS}= (VOUT + 1.6V) or ≥2.7V, C_{IN}=1μF, C_{OUT}=2.2μF , C_{BIAS} =0.1μF)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Input Voltage		VOUT+V_{DO}		5.5	V
V_{BIAS}	Bias Voltage		(VOUT+1.6) or≥2.6		5.5	V
V_{FB}	Feedback Voltage	Adjustable Voltage I_{OUT}=1mA	0.792	0.8	0.808	V
VOUT	Output Voltage	Fixed Voltage I_{OUT}=1mA	0.99* VOUT	VOUT	1.01* VOUT	V
I_{LIM}	Current Limit		600		1000	mA
VIN_{LINE}	VIN Line Regulation	V_{IN}=(VOUT+0.5V) to 5.5V, I_{OUT}=1mA		0.01	0.1	%/V
$VBIAS_{LINE}$	VBIAS Line Regulation	2.7 V or (VOUT(NOM) + 1.6 V), whichever is greater < VBIAS < 5.5 V		0.01	0.1	%/V
V_{DO}	VIN Dropout Voltage[3]	IOUT = 150mA, VOUT falls 3% below VOUT(NOM)		40	50	mV
		IOUT = 500 mA, VOUT falls 3% below VOUT(NOM)		150	200	mV
V_{DO}	BIAS Dropout Voltage[3]	IOUT = 500 mA, VOUT falls 3% below VOUT(NOM)		1.2	1.8	V
Reg_{LOAD}	Load Regulation	I_{OUT}=1~500mA		15	70	mV
I_{BIAS}	Bias Pin Operating Current	VBIAS = 2.7 V		70	90	μA
$I_{BIAS(DIS)}$	Bias Pin Disable Current	VEN ≤ 0.4 V		0.01	1	μA
$I_{VIN(DIS)}$	VIN Pin Disable Current	VEN ≤ 0.4 V		0.01	1	μA
$PSRR_{(VIN)}$	Power Supply Rejection Ratio	VIN to VOUT, f = 1 kHz, VOUT(nom)=V_{FB}，IOUT = 150 mA, VIN ≥ VOUT +0.5 V		70		dB
$PSRR_{(BIAS)}$	Power Supply Rejection Ratio	VBIAS to VOUT, f = 1 kHz, VOUT(nom)=V_{FB}，IOUT = 150 mA, VIN ≥ VOUT +0.5 V		78		dB
e_n	Output Voltage Noise	VIN = VOUT +0.5 V, VOUT(NOM) = 1 V, f = 10 Hz to 100 kHz		60		$μV_{RMS}$
V_{IH}	EN Input Logic High	EN Input Voltage High	1.2			V
V_{IL}	EN Input Logic Low	EN Input Voltage Low			0.4	V
I_{EN}	EN Pull Down Current	VEN = 5.5 V		0.3	1	μA
TSHDN	Thermal Shutdown Temperature			160		°C
TSDH	Thermal Shutdown Hysteresis			20		°C
RDISCH	Output Discharge Pull-Down			220		Ω

Notes:

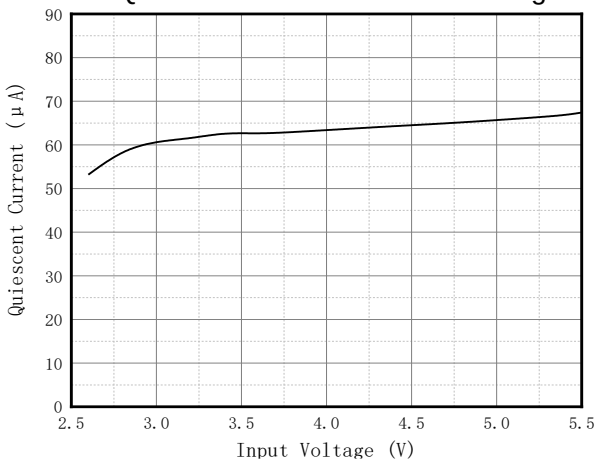
3.1. Dropout voltage is characterized when VOUT falls 3% below VOUT(NOM).

3.2. For output voltages below 1.3V, V_{BIAS} dropout voltage does not apply due to a minimum bias operating voltage of 2.6V.

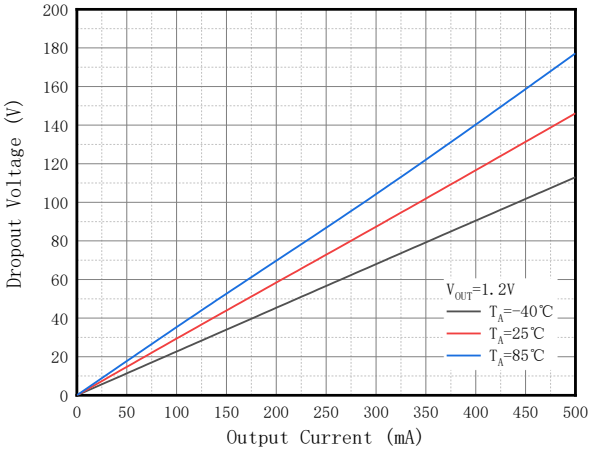
■ Typical characteristics

(Unless otherwise noted, test values are at T_A=25°C, V_{IN}= VOUT + 0.3V, V_{BIAS}=2.7V or VOUT + 1.6V C_{IN}=1μF, C_{OUT}=2.2μF , C_{BIAS}=0.1μF)

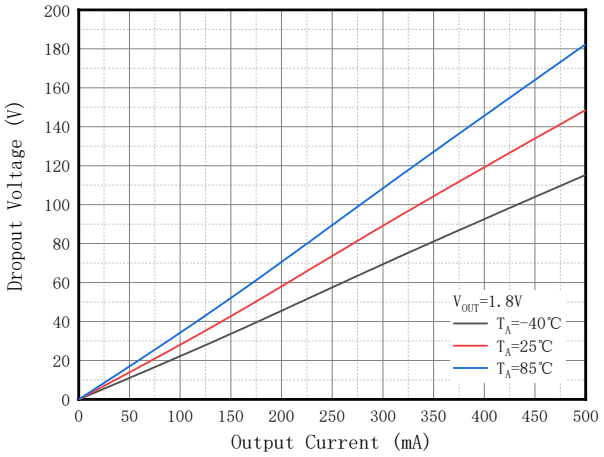
Quiescent Current VS. Bias Voltage



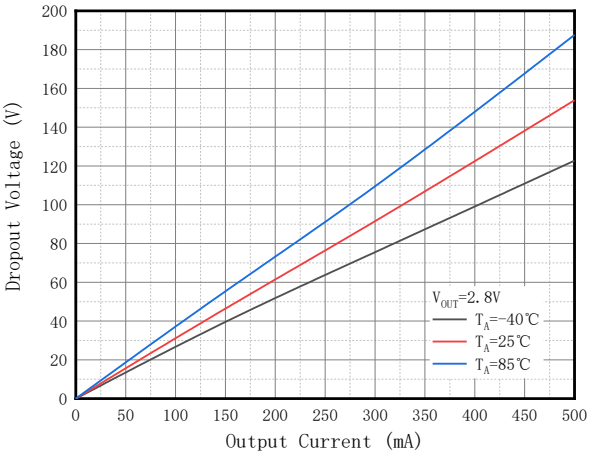
Dropout Voltage Vs. Output Current



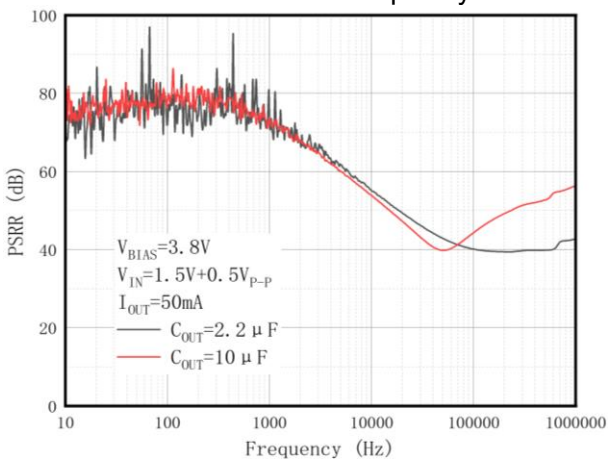
Dropout Voltage Vs. Output Current



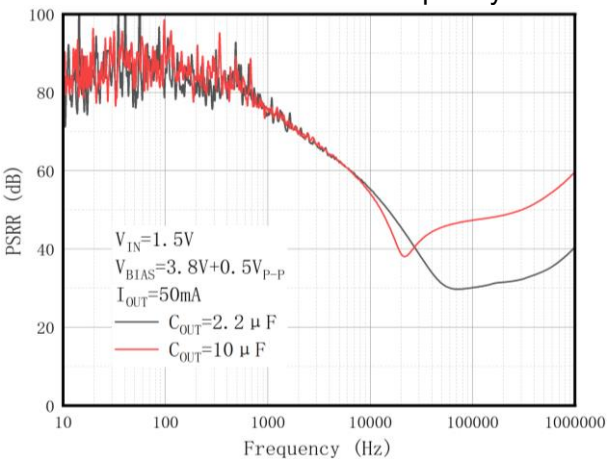
Dropout Voltage Vs. Output Current



VIN-PSRR Vs. Frequency



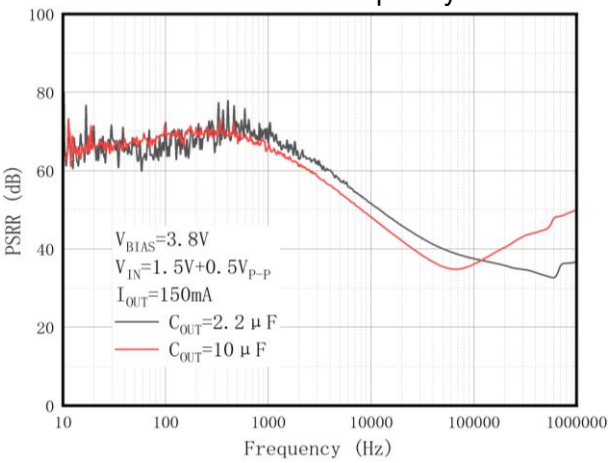
VBIAS-PSRR Vs. Frequency



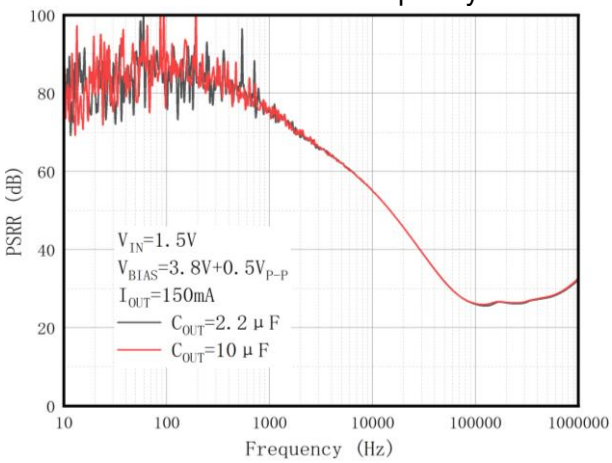
Typical characteristics

(Unless otherwise noted, test values are at T_A=25°C, V_{IN}= VOUT + 0.3V, V_{BIAS}=2.7V or VOUT + 1.6V C_{IN}=1μF, C_{OUT}=2.2μF , C_{BIAS}=0.1μF)

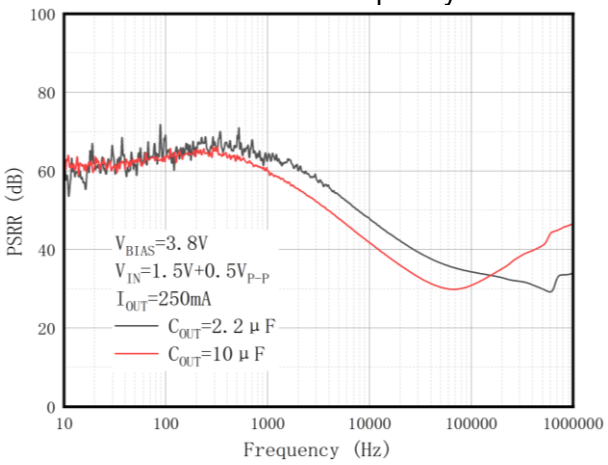
VIN-PSRR Vs. Frequency



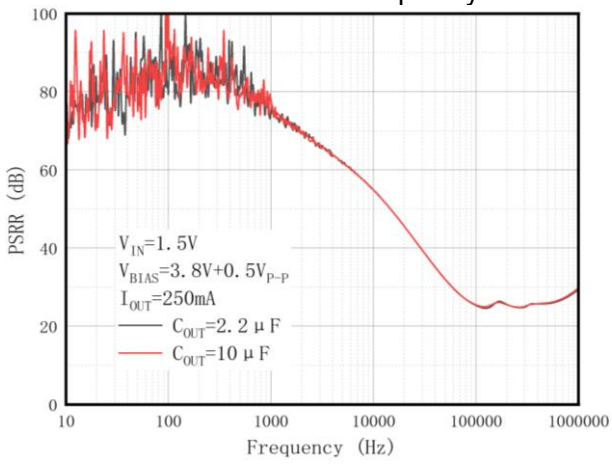
VBIAS-PSRR Vs. Frequency



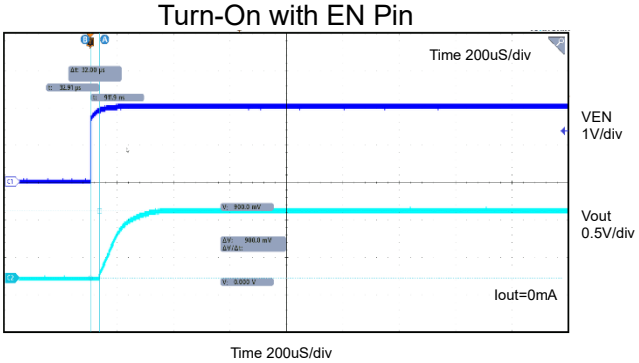
VIN-PSRR Vs. Frequency



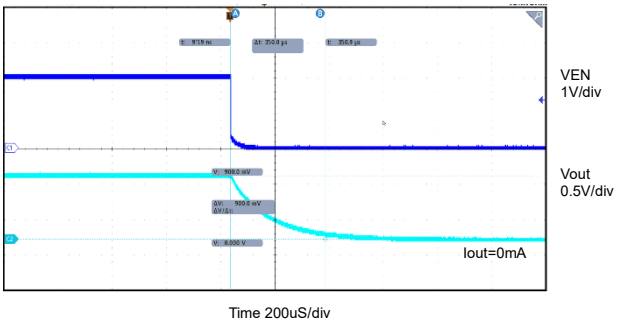
VBIAS-PSRR Vs. Frequency



Turn-On with EN Pin



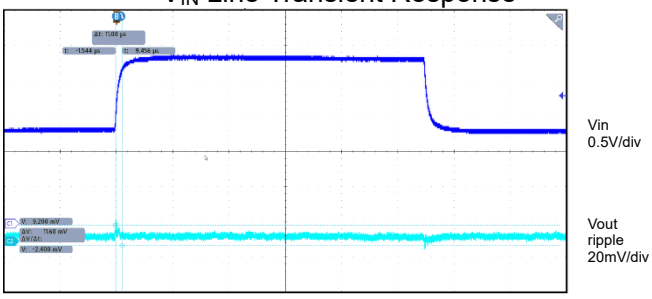
Turn-Off with EN Pin



Typical characteristics

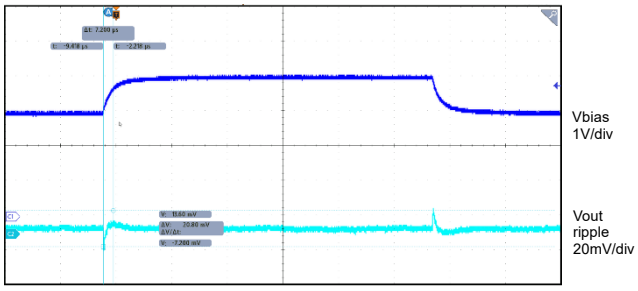
(Unless otherwise noted, test values are at T_A=25°C, V_{IN}= VOUT + 0.3V, V_{BIAS}=2.7V or VOUT + 1.6V C_{IN}=1μF, C_{OUT}=2.2μF , C_{BIAS}=0.1μF)

V_{IN} Line Transient Response



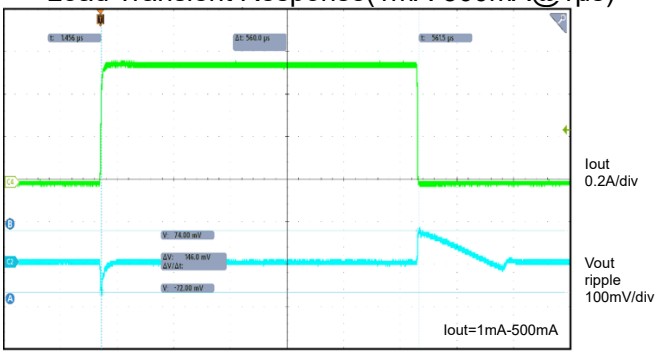
Time 100uS/div

V_{BIAS} Line Transient Response



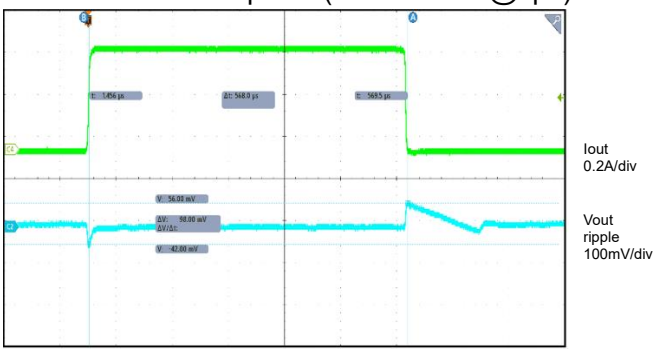
Time 40uS/div

Load Transient Response(1mA-500mA@1μs)



Time 100uS/div

Load Transient Response(1mA-500mA@5μs)



Time 100uS/div

■ Application Information

The OCP1405 dual-rail very low dropout voltage regulator is using NMOS pass transistor for output voltage regulation from VIN voltage. All the low current internal control circuitry is powered from the VBIAS voltage. The use of an NMOS pass transistor offers several advantages in applications. Unlike PMOS topology devices, the output capacitor has reduced impact on loop stability. V_{IN} to VOUT operating voltage difference can be very low compared with standard NMOS regulators in very low Vin applications. The OCP1405 offers smooth monotonic start-up. The controlled voltage rising limits the inrush current. The Enable (EN) input is equipped with internal hysteresis. OCP1405 Voltage linear regulator Fixed version is available

Input Capacitor:

A 1μF ceramic capacitor is recommended to connect VIN pin as close as possible which is used to provide low impedance path to unwanted signal or noise. Larger input capacitor may be necessary if fast and large load transients are encountered in the application. For PCB layout, a wide copper trace is required for both VIN and GND.

Output Capacitor:

The output capacitor is required for the LDO stability. The recommended output capacitance is from 1μF to 4.7μF, Place output capacitor as close as possible to VOUT pin.

Output Voltage Setting:

The required output voltage of adjustable devices can be adjusted from 0.8V to 3.6V using two external resistors. Typical application circuit is shown in Figure 6.

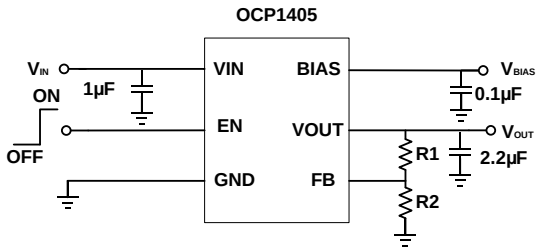


Figure 6. Typical Application Circuit

Choose R2 = 40kΩ to maintain a 20μA minimum load. Calculate the value for VOUT using the following equation:

$$VOUT = VFB \times \left[\frac{R1}{R2} + 1\right]$$

Where: VFB = 0.8V;

Dropout Voltage:

Because of two power supply inputs VIN and VBIAS and one VOUT regulator output, there are two Dropout voltages specified. The first, the VIN Dropout voltage is the voltage difference (VIN – VOUT) when VOUT starts to decrease by percent specified in the Electrical Characteristics table. VBIAS is high enough; specific value is published in the Electrical Characteristics table. The second, VBIAS dropout voltage is the voltage difference (VBIAS – VOUT) when VIN and VBIAS pins are joined together and VOUT starts to decrease.

Enable Operation:

The enable pin will turn the regulator on or off. The threshold limits are covered in the electrical characteristics table in this data sheet. If the enable function is not to be used then the pin should be connected to VIN or VBIAS.

Current Limitation:

The internal Current Limitation circuitry allows the device to supply the full nominal current and surges but protects the device against Current Overload or Short.

Thermal Protection:

Internal thermal shutdown (TSD) circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When TSD activated, the regulator output turns off. When cooling down under the low temperature threshold, device output is activated again. This TSD feature is provided to prevent failures from accidental overheating.

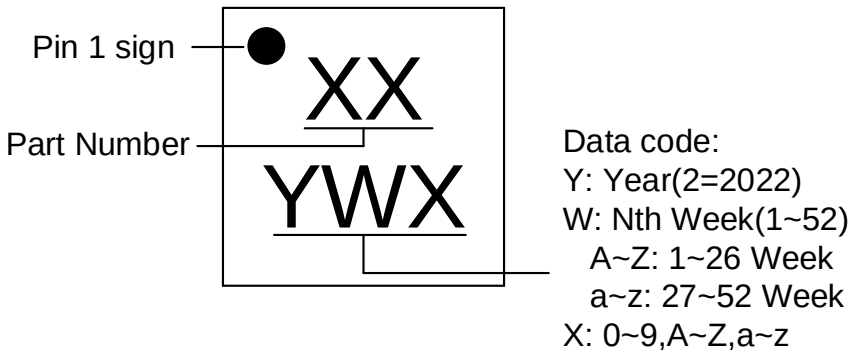
Activation of the thermal protection circuit indicates excessive power dissipation or inadequate heatsinking. For reliable operation, junction temperature should be limited to +125°C maximum.

■ Ordering Information

Part Number	VOUT(V)	V_{FB}(V)	Marking	Package Type	Package Qty	Temperature	Eco Plan	Lead
OCP1405V600AD	ADJ	0.8	CF	DFN1212-6L	3000pcs	-40～85℃	Green	Sn
OCP1405V609AD	0.9	-	CG	DFN1212-6L	3000pcs	-40～85℃	Green	Sn

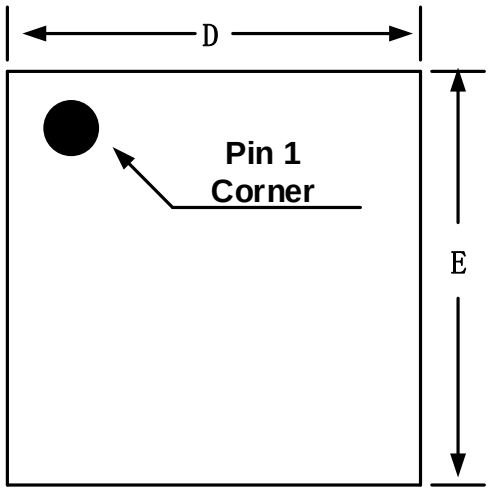
■ Marking Information

DFN1212-6L

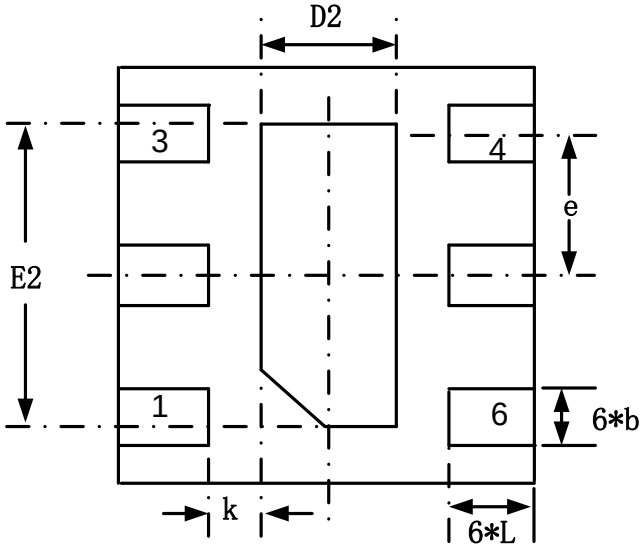


■ Package Information

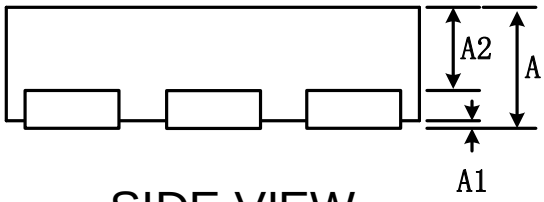
DFN1212-6L



TOP VIEW



BOTTOM VIEW

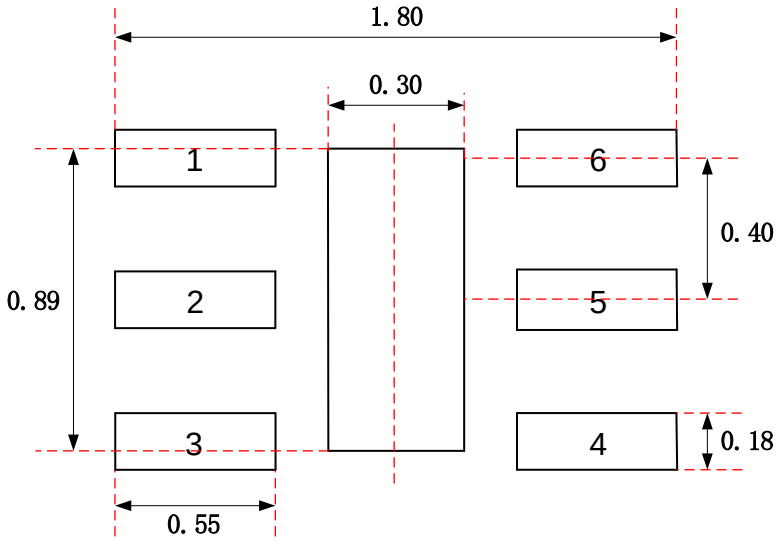


SIDE VIEW

Symbol	Dimensions In Millimeters		
	Min.	Nom.	Max.
A	0. 40	0.45	0.50
A1	0.00	0.02	0.05
A2	-	0.325	-
b	0.13	0.18	0.23
D		1.2 BSC	
E		1.2 BSC	
e		0.4 BSC	
D2	0.25	0.30	0.35
E2	0.84	0.89	0.94
L	0.20	0.25	0.30
K		0.20 REF	

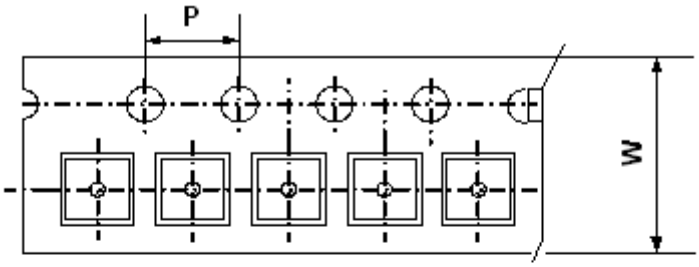
■ Land Pattern Data

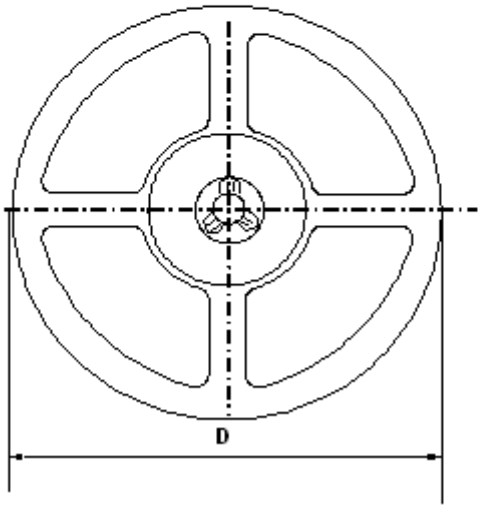
DFN1212-6L



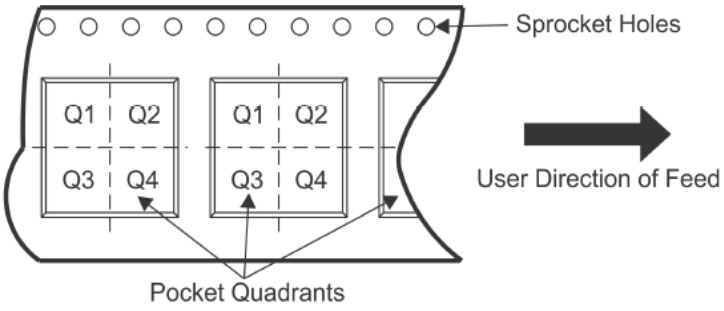
NOTE: All dimensions are in millimeters(mm).

■ Packing Information





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Package Type	Carrier Width(W)	Pitch(P)	Reel Size(D)	Packing Minimum	PIN 1 Quadrant	MSL
DFN1212-6L	8±0.1 mm	4±0.1 mm	180±1 mm/7’	3000pcs	Q1	Level-3

Note: Carrier Tape Dimension, Reel Size and Packing Minimum

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