■ General Description

OCP96011 is a high-performance USB Type−C port multimedia switch which supports USB2.0 signal, analog audio, sideband use wires and analog microphone signal. OCP96011 also supports high voltage on SBUx signal and USB signal on USB Type−C receptacle side.

The device is a RoHS compliant 25-Ball 2.23mm x 2.27mm WLCSP.

■ Features

- Wide 2.7V to 5.5V Operating Input Range
- USB Switch
  - SDD_{21} -3dB bandwidth: 1000MHz
  - Ron: 3Ω (Typ.)
- Audio Switch
  - Signal range: -3V to +3V
  - THD+N=-108dB @ 32Ω,1Vrms, f=20Hz~20kHz
  - Ron: 1Ω (Typ.)
- High Voltage Protection
  - 20.5V DC tolerance on connector side Pins
  - Over voltage protection
- OMTP and CTIA Pinout Support
- Available in 25-Ball WLCSP
- -40℃ to +85℃ Operating Temperature Range

■ Applications

- Mobile-phones
- Tablets
- Notebook

■ Pin Configuration

WLCSP-25 (Top View)

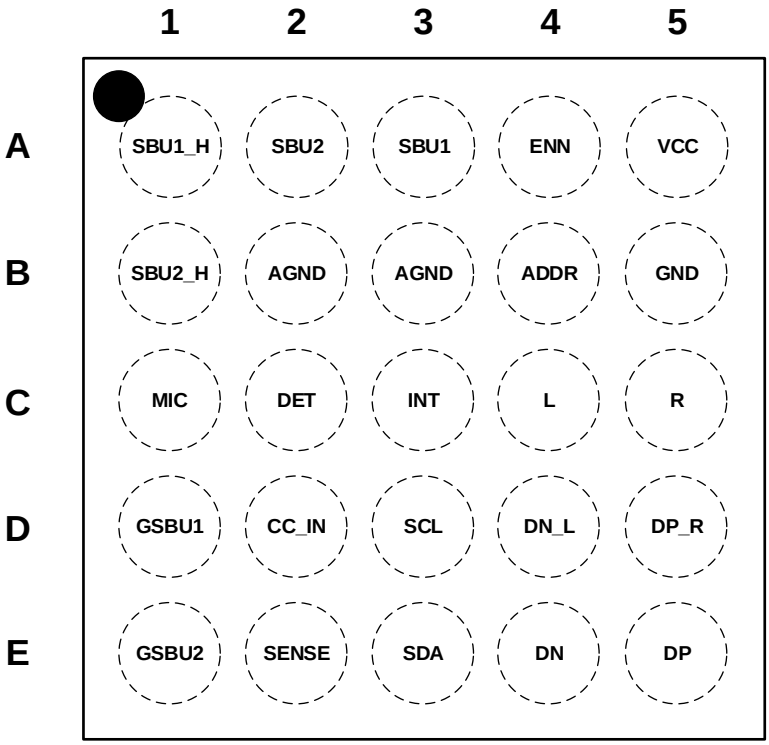


Figure 1, Pin Assignments of OCP96011

■ Pin Descriptions

Pin	Pin Name	Pin Function
A1	SBU1_H	Host Side Sideband Use Wire 1
A2	SBU2	Sideband use wire 2
A3	SBU1	Sideband use wire 1
A4	ENN	Chip Enable, active low, internal pull-down by 470 k
A5	VCC	Power Supply (2.7 to 5.5 V)
B1	SBU2_H	Host Side Sideband Use Wire 2
B2, B3	AGND	Audio signal ground
B4	ADDR	I2C slave address pin
B5	GND	Chip ground
C1	MIC	Microphone signal
C2	DET	Push-pull output. When CC_IN > 1.5 V, DET is low and CC_IN < 1.2 V, DET is high
C3	INT	I2C Interrupt output, active low (open drain)
C4	L	Audio – Left Channel
C5	R	Audio – Right Channel
D1	GSBU1	Audio sense path 1 to headset jack GND
D2	CC_IN	Audio accessory attachment detection input
D3	SCL	I2C clock
D4	DN_L	USB/Audio Common Connector
D5	DP_R	USB/Audio Common Connector
E1	GSBU2	Audio sense path 2 to headset jack GND
E2	SENSE	Audio ground reference output
E3	SDA	I2C data
E4	DN	USB Data (Differential –)
E5	DP	USB Data (Differential +)

■ Typical Application Circuit

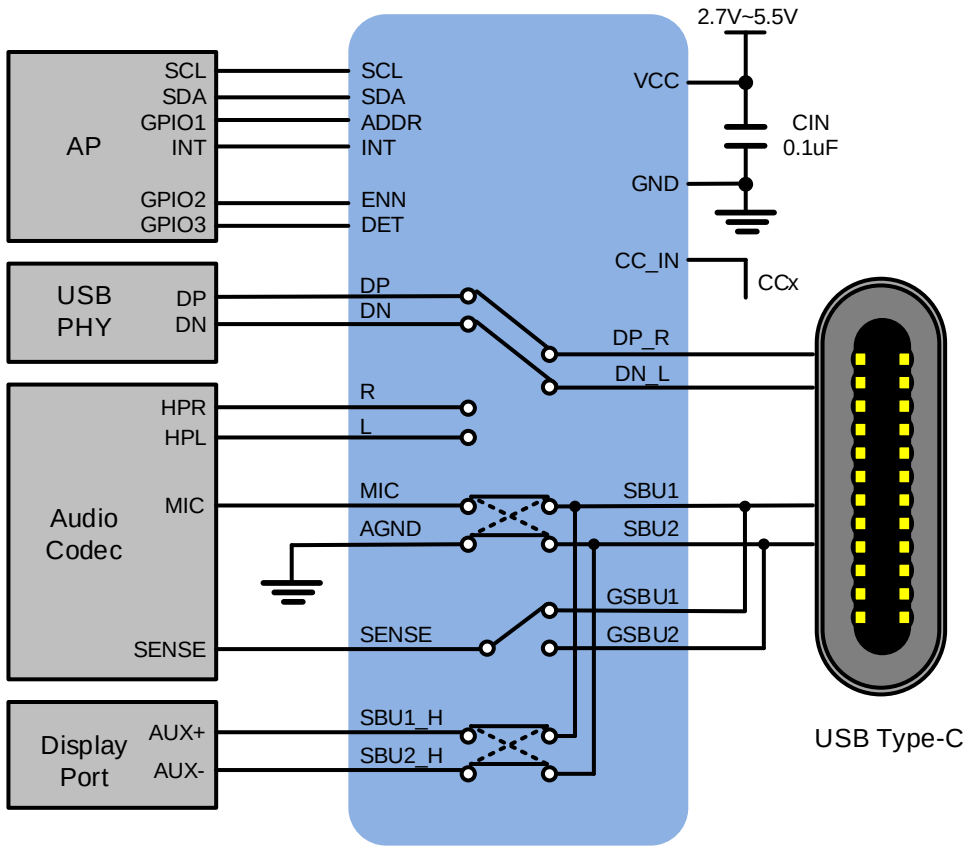


Figure 2, Typical Application Block diagram of OCP96011

■ Absolute Maximum Ratings[1] (T_A=25°C unless otherwise noted)

Parameter	Symbol	Rating	Unit
Supply Voltage from VCC	V_{CC}	-0.3 to 6.5	V
V_{CC_IN} to GND	V_{CC_IN}	-0.3 to 20.5	V
V_{SBU1} to GND, V_{SBU2} to GND, V_{GSBU1} to GND, V_{GSBU1} to GND	$V_{V\_SBU/GSBU}$	-0.3 to 20.5	V
V_{DP_R} to GND, V_{DN_L} to GND	V_{SW_C}	-3.5 to 20.5	V
V_{DP} to GND, V_{DN} to GND	V_{SW_USB}	-0.3 to 6.5	V
V_L to GND, V_R to GND	V_{SW_Audio}	-3.6 to 6.5	V
V_{SBU1_H} to GND, V_{SBU2_H} to GND	V_{VSBU_H}	-0.3 to 6.5	V
SENSE, MIC, DET, INT, to GND	$V_{I/O}$	-0.3 to 6.5	V
SDA, SCL, ENN, ADDR to GND	V_{CNTRL}	-0.3 to 6.5	V
Switch I/O Current, Audio Path	I_{SW_Audio}	-250 to 250	mA
Switch I/O Current, USB Path	I_{SW_USB}	100	mA
Switch I/O Current, MIC to SBU1 or SBU2	I_{SW_MIC}	50	mA
Switch I/O Current, SBUx to SBUx_H	I_{SW_SBU}	50	mA
Switch I/O Current, SENSE to GSBU1 or GSBU2	I_{SW_SENSE}	100	mA
Switch I/O Current, AGND to SBU1 or SBU2	I_{SW_AGND}	500	mA
Human Body model of VCC, SBU1, SBU2, DP_R, DN_L, GSBU1, GSBU2, CC_IN	HBM	4	kV
Human Body model of Host side pins		2	kV
Charged Device Model	CDM	1	kV
Storage Temperature Range	T_S	-55 to +150	℃
Maximum Operating Junction Temperature Range	T_J	-40 to 125	℃

Notes: 1)Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

■ Recommended Operating Conditions2(TA=25°C unless otherwise noted)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	2.7 ~ 5.5	V
USB SWITCH			
V_{DP} to GND, V_{DN} to GND, V_{DP_R} to GND, V_{DN_L} to GND	V_{SW_USB}	0 ~ +3.6	V
AUDIO SWITCH			
V_{DP_R} to GND, V_{DN_L} to GND, V_L to GND, V_R to GND	V_{SW_Audio}	-3.6 ~ +3.6	V
MIC SWITCH			
V_{SBU1} to GND, V_{SBU2} to GND, V_{MIC} to GND	V_{VSBUX_MIC}	0 ~ +3.6	V
SENSE SWITCH			
V_{GSBU1} to GND, V_{GSBU2} to GND, V_{SENSE} to GND	V_{VGSBUX_SENSE}	0 ~ +3.6	V
SBUX TO SBUX_H SWITCH			
V_{SBU1} to GND, V_{SBU2} to GND, V_{SBU1_H} to GND, V_{SBU2_H} to GND	$V_{VSBUX\_SBUX\_H}$	0 ~ +3.6	V
CC_IN PIN			
V_{CC_IN} to GND	V_{CC_IN}	0 ~ +5.5	V
CONTROL VOLTAGE (ENN/SDA/SCL)			
Input Voltage High	V_{IH}	1.3 ~ VCC	V
Input Voltage Low	V_{IL}	0 ~ 0.45	V
OPERATING TEMPERATURE			
Ambient Operating Temperature	T_A	-40 to 85	℃

Notes: 2) The device is not guaranteed to function outside of its operating conditions

■ Electrical Characteristics

(Unless otherwise noted, typical values are at T_A=25℃, V_{CC}=3.3V)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power consumption						
I_{CC}	Supply Current	V_{CC}: 2.7 V to 5.5 V; USB switches on, SBUx to SBUx_H switches on			65	μA
		V_{CC}: 2.7 V to 5.5 V; Audio switches on, MIC switches on and Audio GND switch on			60	μA
I_{CCZ}	Quiescent Current	ENN = L, 04H'b7 = 0			5	μA
USB/AUDIO COMMON PINS: DP_R, DN_L						
I_{OZ}	Off Leakage Current of DP_R and DN_L	V_{CC}: 2.7 V to 5.5 V; DN_L, DP_R = -3 V to 3.6 V	3.0		3.0	μA
I_{OFF}	Power-Off Leakage Current of DP_R and DN_L	V_{CC}: 0V; DN_L, DP_R = 0 V to 3.6 V	3.0		3.0	μA
V_{OV_TRIP}	OVP threshold	V_{CC}: 2.7 V to 5.5 V; Rising edge	4.5	5	5.3	V
V_{OV_HYS}	OVP Hysteresis	V_{CC}: 2.7 V to 5.5 V;		0.3		V
Audio Switch						
I_{ON}	Audio switch on leakage current	V_{CC}: 2.7 V to 5.5 V; DN_L, DP_R = -3 V to 3 V; DP, DN, R, L = Float	-2.5		2.5	μA
I_{OFF}	Power-Off Leakage Current of L and R	V_{CC}: 0 V L, R = 0V to 3 V; DP_R, DN_L, = Float	-1.0		1.0	μA
R_{ON_AUDIO}	Audio Switch On Resistance	V_{CC}: 2.7 V to 5.5 V; I_{SW} = 100 mA, V_{SW} = -3V to 3 V		1.0	2.0	Ω
R_{SHUNT}	Pull Down Resistor on R/L Pin when Audio Switch is Off	V_{CC}: 2.7 V to 5.5 V; L = R = 3 V	6	10	14	kΩ
USB Switch						
I_{ON}	USB switch on leakage current	V_{CC}: 2.7 V to 5.5 V; DN_L, DP_R = 0 V to 3.6V; DP, DN, R, L = Float	-3.0		3.5	μA
I_{OZ}	Off Leakage Current of DP and DN	V_{CC}: 2.7 V to 5.5 V; DN, DP= 0 V to 3.6 V	-3.0		3.0	μA
I_{OFF}	Power-Off Leakage Current of DP and DN	V_{CC}: 0V; DN, DP= 0 V to 3.6 V	-3.0		3.0	μA
R_{ON_USB}	USB Switch On Resistance	V_{CC}: 2.7 V to 5.5 V; I_{SW} = 8 mA, V_{SW} = 0.4 V		3.0	5.0	Ω
SENSE Switch						
I_{ON}	SENSE switch on leakage current	V_{CC}: 2.7 V to 5.5 V; GSBUx = 0 V to 1 V, SENSE is floating.	-2.0		2.0	μA
I_{OZ}	Off Leakage Current of SENSE Pin	V_{CC}: 2.7 V to 5.5 V; Sense= 0 V to 1 V	-2.0		2.0	μA
	Off Leakage Current of GSBUx Pin	V_{CC}: 2.7 V to 5.5 V; GSBUx= 0 V to 1 V	-2.0		2.0	μA
		V_{CC}: 2.7 V to 5.5 V; GSBUx= 1 V to 3.6 V	-3.0		3.0	μA
I_{OFF}	Power-Off Leakage Current of SENSE Pin	V_{CC}: 0V; Sense= 0 V to 1 V	-2.0		2.0	μA
	Power-Off Leakage Current of GSBUX Pin	V_{CC}: 0V; GSBUx= 0 V to 3.6 V	-3.0		3.0	μA
R_{ON_SENSE}	SENSE Switch On Resistance	V_{CC}: 2.7 V to 5.5 V; I_{SW} = 100 mA, V_{SW} = 1 V	0.2	0.3	0.4	Ω
V_{OV_TRIP}	OVP threshold of GSBUx	V_{CC}: 2.7 V to 5.5 V; Rising edge	4.5	5	5.3	V
V_{OV_HYS}	OVP Hysteresis of GSBUx	V_{CC}: 2.7 V to 5.5 V;		0.35		V

■ Electrical Characteristics

(Unless otherwise noted, typical values are at T_A=25℃, V_{CC}=3.3V)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SBUX PINS						
I_{OZ}	Off Leakage Current of SBUx	V_{CC}: 2.7 V to 5.5 V; SBUx= 0 V to 3.6 V	3.0		3.0	μA
I_{OFF}	Power-Off Leakage Current of SBUx	V_{CC}: 0 V; SBUx= 0 V to 3.6 V	3.0		3.0	μA
V_{OV_TRIP}	OVP threshold	V_{CC}: 2.7 V to 5.5 V; Rising edge	4.5	5	5.3	V
V_{OV_HYS}	OVP Hysteresis	V_{CC}: 2.7 V to 5.5 V;		0.35		V
MIC Switch						
I_{ON}	MIC switch on leakage current	V_{CC}: 2.7 V to 5.5 V; SBUx = 0 V to 3.6 V; MIC = Float	-3.0		3.0	μA
I_{OZ}	Off Leakage Current of MIC	V_{CC}: 2.7 V to 5.5 V; MIC = 0V to 3.6 V;	-1.0		1.0	μA
I_{OFF}	Power-Off Leakage Current of MIC	V_{CC}: 0V; MIC = 0V to 3.6 V;	-1.0		1.0	μA
R_{ON_MIC}	MIC Switch On Resistance	V_{CC}: 2.7 V to 5.5 V; I_{SW} = 30 mA, V_{SW} = 3.6 V		3.0	4.0	Ω
SBUx_H Switch						
I_{ON}	SBUx_H switch on leakage current	V_{CC}: 2.7 V to 5.5 V; SBUx = 0 V to 3.6 V; SBUx_H = Float	-3.0		3.0	μA
I_{OZ}	Off Leakage Current of SBUx_H	V_{CC}: 2.7 V to 5.5 V; SBUx_H= 0 V to 3.6 V	-1.0		1.0	μA
I_{OFF}	Power-Off Leakage Current of SBUx_H	V_{CC}: 0V; SBUx_H= 0 V to 3.6 V	-1.0		1.0	μA
$R_{ON\_SBUX\_H}$	SBUx_H Switch On Resistance	V_{CC}: 2.7 V to 5.5 V; I_{SW} = 30 mA, V_{SW} = 0 V to 3.6 V		3.0	4.0	Ω
Audio Ground Switch						
R_{ON_AGND}	AGND Switch On Resistance	V_{CC}: 2.7 V to 5.5 V; I_{SW} = 100 mA		60	90	mΩ
CC_IN						
V_{TH_L}	Input Low Threshold	V_{CC}: 2.7 V to 5.5 V		1.2		V
V_{TH_H}	Input High Threshold	V_{CC}: 2.7 V to 5.5 V		1.5		V
$I_{IN\_CC\_IN}$	CC_IN input leakage	V_{CC}: 2.7 V to 5.5 V; CC_IN=0V to 5.5V			1.0	μA
ENN						
V_{IH}	Input Voltage High	V_{CC}: 2.7 V to 5.5 V	1.3			V
V_{IL}	Input Voltage Low	V_{CC}: 2.7 V to 5.5 V			0.45	V
R_{PD}	Internal Pull Down Resistor	V_{CC}: 2.7 V to 5.5 V		470		kΩ
ADDR						
V_{TH_H}	Input High Threshold	V_{CC}: 2.7 V to 5.5 V	1.3			V
V_{TH_L}	Input Low Threshold	V_{CC}: 2.7 V to 5.5 V			0.45	V
I_{IN_ADDR}	ADDR input leakage	V_{CC}: 2.7 V to 5.5 V; ADDR=0V to VCC	-1.0		1.0	μA
INT/DET						
V_{OH}	Output Voltage High for DET	V_{CC}: 2.7 V to 5.5 V; Io = -2 mA	1.5			V
V_{OL}	Output Voltage Low for DET and INT	V_{CC}: 2.7 V to 5.5 V; Io = -2 mA			0.4	V
SCL/SDA						
V_{IL_I2C}	Low-Level Input Voltage	V_{CC}: 2.7 V to 5.5 V			0.4	V
V_{IH_I2C}	High-Level Input Voltage	V_{CC}: 2.7 V to 5.5 V	1.2			V
V_{OL_SDA}	Low-Level Output VoltageS	V_{CC}: 2.7 V to 5.5 V; I_{OL} = 2 mA			0.3	V
I_{OL_SDA}	Low-Level Output Current	V_{CC}: 2.7 V to 5.5 V; V_{OL_SDA} = 0.2 V	10			mA
I_{I2C}	Input Current of SDA and SCL Pins	V_{CC}: 2.7 V to 5.5 V; SCL/SDA = 0 V to 3.6 V	-2.0		2.0	μA

■ AC Electrical Characteristics

(Unless otherwise noted, typical values are at T_A=25℃, V_{CC}=3.3V)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Audio Switch						
t_{delay}	Audio Switch Turn On Delay Time	DP_R = DN_L = 1 V, R_L = 32Ω		45		μs
t_{rise}	Audio Switch Turn On Rising Time[3]	DP_R = DN_L = 1 V, R_L = 32Ω		325		μs
t_{OFF}	Audio Switch Turn Off Time	DP_R = DN_L = 1 V, R_L = 32Ω		10		μs
X_{TALK}	Cross Talk (Adjacent)	f = 1 kHz, R_L = 50Ω, V_{SW} = 1 V_{RMS}		-105		dB
O_{IRR}	Off Isolation	f= 1 kHz, R_L = 50Ω, V_{SW} = 1 V_{RMS}, C_F=0pF		-105		dB
THD+N	Total Harmonic Distortion + Noise Performance with A-weighting Filter	R_L = 600Ω, f = 20Hz~20kHz, V_{SW} = 1.4 V_{RMS}		-108		dB
		R_L = 32Ω, f = 20Hz~20kHz, V_{SW} = 1 V_{RMS}		-108		dB
		R_L = 16Ω, f = 20 Hz~20kHz, V_{SW} = 0.5 V_{RMS}		-108		dB
BW	-3 dB Bandwidth	R_L = 50Ω		650		MHz
USB Switch						
t_{ON}	USB Switch Turn On Time	DP_R = DN_L = 1.5 V, R_L = 50Ω		20		μs
t_{OFF}	USB Switch Turn Off Time	DP_R = DN_L = 1.5 V, R_L = 50Ω		7		μs
O_{IRR}	Off Isolation between DP, DN and Common Node Pins	f= 1 kHz, R_L = 50Ω, V_{SW} = 1 V_{RMS}, C_F=0pF		-100		dB
BW	SDD_{21} -3 dB Bandwidth	R_L = 50Ω		1000		MHz
t_{OVP}	DP_R and DN_L pins OVP Response Time	Vsw = 3.5 V to 5.5 V		1	1.5	μs
MIC/Audio Ground Switch						
T_{delay}-MIC	MIC Switch Turn On Delay Time	SBUx = 1 V; R_L = 50Ω		50		μs
T_{rise}-MIC	MIC Switch Turn On Rising Time[5]	SBUx = 1 V; R_L = 50Ω		450		μs
T_{delay}-AGND	AGND Switch Turn On Delay Time	SBUx pulled up to 0.5 V by 16Ω, AGND connect to GND		70		μs
T_{rise}-AGND	AGND Switch Turn On Rising Time[5]	SBUx pulled up to 0.5 V by 16Ω, AGND connect to GND		3000		μs
T_{OFF}_MIC	MIC Switch Turn Off Time	SBUx = 2.5 V, R_L = 50Ω		10		μs
T_{OFF}_AGND	AGND Switch Turn Off Time	SBUx: Isource = 10 mA, clamp to 2.5 V		8		μs
BW	-3 dB Bandwidth	R_L = 50Ω		30		MHz
SBUx_H Switch						
t_{ON}	SBUx_H Switch Turn On Time	SBUx = 2.5 V, R_L = 50Ω		60		μs
t_{OFF}	SBUx_H Switch Turn Off Time	SBUx = 2.5 V, R_L = 50Ω		7		μs
BW	-3 dB Bandwidth	R_L = 50Ω		30		MHz
t_{OVP}	SBUx pins OVP Response Time	Vsw = 3.5 V to 5.5 V		0.5	1	μs
SENSE Switch						
$t_{delay\_}$	Sense Switch Turn On Delay Time	GSBUx = 1 V, RL = 50Ω		55		μs
t_{rise}	Sense Switch Turn On Rising Time (Note1)	GSBUx = 1 V, RL = 50Ω		350		μs
t_{OFF}	Sense Switch Turn Off Time	GSBUx = 1 V, RL = 50Ω		5		μs
BW	-3 dB Bandwidth	RL = 50Ω		150		MHz
t_{OVP}	GSBUx pins OVP Response Time	Vsw = 3.5 V to 5.5 V		0.5	1.5	μs
DTE Delay						
t_{delay} _DET	DET Response Delay	Transition from 0 to 1.8 V		0.5		μs
		Transition from 1.8 to 0 V		2		μs

Notes: 3) Turn on timing can be controlled by I2C register

■ I2C SPECIFICATION

I²C Compatible Timing Specifications (SCL, SDA), see Figure 4

Symbol	Parameter	Mode	Min.	Typ.	Max.	Unit
f_{SCL}	SCL clock frequency	Standard Mode	-	-	100	KHz
		Fast Mode	-	-	400	KHz
t_{LOW}	Low period of the SCL clock	Standard Mode	4.7	-	-	μs
		Fast Mode	1.3	-	-	μs
t_{HIGH}	High period of the SCL clock	Standard Mode	4.0	-	-	μs
		Fast Mode	0.6	-	-	μs
t_{BUF}	Bus free time between a STOP and START condition	Standard Mode	4.7	-	-	μs
		Fast Mode	1.3	-	-	μs
$t_{HD,STA}$	Hold time for a repeated START condition	Standard Mode	4.0	-	-	μs
		Fast Mode	0.6	-	-	μs
$t_{SU,STA}$	Setup time for a repeated START condition	Standard Mode	4.7	-	-	μs
		Fast Mode	0.6	-	-	μs
$t_{SU,DAT}$	Data setup time	Standard Mode	0.25	-	-	μs
		Fast Mode	0.1	-	-	μs
$t_{HD,DAT}$	Data hold time	Standard Mode	0.05	-	3.45	μs
		Fast Mode	0.05	-	0.9	μs
t_{RCL1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	Standard Mode	20+0.1CB	-	1000	ns
		Fast Mode	20+0.1CB	-	1000	ns
t_{RCL}	Rise time of SCL signal	Standard Mode	20+0.1CB	-	1000	ns
		Fast Mode	20+0.1CB	-	300	ns
t_{FCL}	Fall time of SCL signal	Standard Mode	20+0.1CB	-	300	ns
		Fast Mode	20+0.1CB	-	300	ns
t_{RDA}	Rise time of SDA signal	Standard Mode	20+0.1CB	-	1000	ns
		Fast Mode	20+0.1CB	-	300	ns
t_{FDA}	Fall time of SDA signal	Standard Mode	20+0.1CB	-	300	ns
		Fast Mode	20+0.1CB	-	300	ns
$t_{SU,STO}$	Setup time for STOP condition	Standard Mode	4.0	-	-	μs
		Fast Mode	0.6	-	-	μs
CB	Capacitive load for SCL and SDA		-	-	0.4	nF

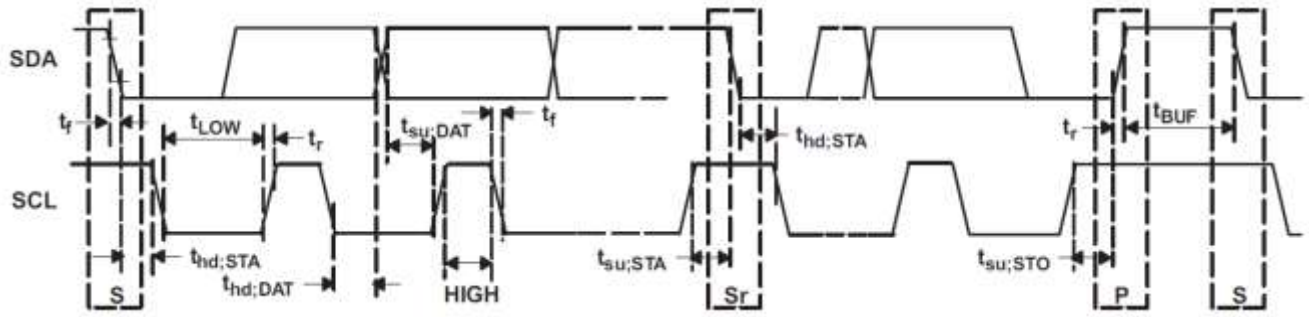


Figure3, Serial Interface Timing for F/S-Mode I²C

■ Capacitance Characteristics4

(Unless otherwise noted, typical values are at T_A=25℃, V_{CC}=3.3V)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$C_{ON\_USB/Audio}$	On Capacitance (Common Port)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias		11		pF
$C_{OFF\_USB/Audio}$	Off Capacitance (Common Port)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias		8		pF
C_{OFF_USB}	Off Capacitance (Non-Common Ports)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias		3		pF
$C_{ON\_SENSE\_SW}$	On Capacitance (Common Ports)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias		45		pF
$C_{OFF\_SENSE\_SW}$	Off Capacitance (Common Ports)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias		100		pF
$C_{ON\_MIC\_SW}$	On Capacitance (Common Ports)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias		100		pF
$C_{OFF\_MIC\_SW}$	Off Capacitance (Common Ports)	f = 1 MHz, 100 mVV_{PK-PK}, 100 mV DC bias		8		pF
$C_{ON\_AGND\_SW}$	On Capacitance (Common Ports)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias		125		pF
$C_{ON\_SBUx\_H\_SW}$	Off Capacitance (Common Ports)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias		190		pF
C_{ENN}	ENN Pin Capacitance	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias		3		pF

Note. 4) OCP96011 is guaranteed to meet performance specifications over the –40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.

■ I2C Slave address Map

ADDR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADDR = L	1	0	0	0	0	1	0	R/W
ADDR = H	1	0	0	0	0	1	1	R/W

■ Register Maps

ADDR	Register Name	Type	Reset Value	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00H	Device ID	R	0x00	0	0	0	0	0	0	0	0
01H	OVP Interrupt Mask	R/W	0x00	Reserved	Mask OVP interrupt	Mask OVP /DP_R	Mask OVP /DN_L	Mask OVP /SBU1	Mask OVP /SBU2	Mask OVP /GSBU1	Mask OVP /GSBU2
02H	OVP interrupt flag	R/C	0x00	Reserved		DP_R	DN_L	SBU1	SBU2	GSBU	GSBU2
03H	OVP status	R	0x00	Reserved		OVP/ DP_R	OVP/ DN_L	OVP/SBU1	OVP/SBU2	OVP/ GSBU1	OVP/ GSBU2
04H	Switch settings Enable	R/W	0x98	Device control	SBU1_H to SBUx	SBU2_H to SBUx	DN_L to DN or L	DP_R to DP or R	Sense to GSBUx	MIC to SBUx	Audio Ground to SBUx
05H	Switch select	R/W	0x18	Reserved	SBU1_H to SBUx	SBU2_H to SBUx	DN_L to DN or L	DP_R to DP or R	Sense to GSBUx	MIC to SBUx	Audio Ground to SBUx
06H	Switch Status0	R	0x05	Reserved		Sense Switch Status		DP_R Switch Status		DN_L Switch Status	
07H	Switch Status1	R	0x00	Reserved		SBU2 Switch Status			SBU1 Switch Status		
08H	Audio Switch Left Channel turn on Control	R/W	0x01	Audio switch left channel slow control [7:0]							
09H	Audio Switch Right Channel turn on Control	R/W	0x01	Audio switch right channel slow control [7:0]							
0AH	MIC switch turn on control	R/W	0x01	MIC switch right channel slow control [7:0]							
0BH	Sense switch turn on control	R/W	0x01	Sense switch right channel slow control [7:0]							
0CH	Audio Ground Switch turn on Control	R/W	0x01	Audio ground switch right channel slow control [7:0]							

■ Register Maps

ADDR	Register Name	Type	Reset Value	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0DH	Timing Delay between R switch enable and L switch enable	R/W	0x00	Timing Delay between R switch enable and L switch enable control [7:0]							
0EH	Timing Delay between MIC switch enable and L switch enable	R/W	0x00	Timing Delay between MIC switch enable and L switch enable control [7:0]							
0FH	Timing Delay between Sense switch enable and L switch enable	R/W	0x00	Timing Delay between Sense switch enable and L switch enable control [7:0]							
10H	Timing Delay between Audio ground switch enable and L switch enable	R/W	0x00	Timing Delay between Audio ground switch enable and L switch enable control [7:0]							
11H	Audio accessory status	R	0x02	Reserved						CC_IN	DET
12H	Function enable	R/W	0x08	Reserved	DET I/O Control	RES detection range setting	GIPO control	SLOW TURN-ON CONTROLL	MIC auto control	RES detection : auto clear	Audio jack detection : auto clear
13H	RES detection pin setting	R/W	0x00	Reserved					Detection pin select [2:0]		
14H	RES detection value	R	0xFF	R detection value [7:0]							
15H	RES detection interrupt threshold	R/W	0x16	R detection Interrupt resistance threshold [7:0]							
16H	RES detection interval	R/W	0X00	Reserved						Detection interval [1:0]	
17H	Audio jack Status	R	0x01	Reserved				4pole, SBU2 MIC	4pole, SBU1 MIC	3pole	No audio
18H	Detection interrupt	R/C	0x00	Reserved					Audio detection done	RES detection occurred	RES detection done
19H	Detection interrupt Mask	R/W	0x00	Reserved					Audio detection done mask	RES detection occurred mask	RES detection done mask
1AH	Audio detection RGE1	R	0xFF	audio detection value REG1 [7:0]							
1BH	Audio detection RGE2	R	0xFF	audio detection value REG2 [7:0]							
1CH	MIC Threshold DATA0	R/W	0x20	MIC Threshold value DATA0 [7:0]							
1DH	MIC Threshold DATA1	R/W	0xFF	MIC Threshold value DATA1 [7:0]							
1EH	I2C Reset	W/C	0x00	Reserved							I2C reset
1FH	Current Source Setting	R/W	0x07	Reserved				Current Source setting [3:0]			

DEVICE ID
Address: 00H
Reset Value: 8'b 0000_0000
Type: Read

Bits	Name	Size	Description
[7:6]	Vendor ID	2	Vendor ID
[5:3]	Version ID	3	Device Version ID
[2:0]	Revision ID	3	Revision History ID

OVP INTERRUPT MASK
Address: 01H
Reset Value: 8'b 0000_0000
Type: Read/Write

Bits	Name	Size	Description
7	Reserved	1	Do Not Use
6	OVP Interrupt mask control	1	OVP Interrupt function Enable/Disable 0: Controlled by [5:0] bit 1: Mask all connector side pins OVP interrupt
5	DP_R OVP Interrupt mask control	1	0: Do not mask OVP interrupt 1: Mask OVP interrupt
4	DN_L OVP Interrupt mask control	1	0: Do not mask OVP interrupt 1: Mask OVP interrupt
3	SBU1 OVP Interrupt mask control	1	0: Do not mask OVP interrupt 1: Mask OVP interrupt
2	SBU2 OVP Interrupt mask control	1	0: Do not mask OVP interrupt 1: Mask OVP interrupt
1	GSBU1 OVP Interrupt mask control	1	0: Do not mask OVP interrupt 1: Mask OVP interrupt
0	GSBU2 OVP Interrupt mask control	1	0: Do not mask OVP interrupt 1: Mask OVP interrupt

OVP INTERRUPT FLAG
Address: 02H
Reset Value: 8'b 0000_0000
Type: Read Clear

Bits	Name	Size	Description
[7:6]	Reserved	2	Do Not Use
5	DP_R OVP	1	0: OVP event has not occurred 1: OVP event has occurred
4	DN_L OVP	1	0: OVP event has not occurred 1: OVP event has occurred
3	SBU1 OVP	1	0: OVP event has not occurred 1: OVP event has occurred
2	SBU2 OVP	1	0: OVP event has not occurred 1: OVP event has occurred
1	GSBU1 OVP	1	0: OVP event has not occurred 1: OVP event has occurred
0	GSBU2 OVP	1	0: OVP event has not occurred 1: OVP event has occurred

OVP STATUS
Address: 03H

Reset Value: 8'b 0000_0000
Type: Read

Bits	Name	Size	Description
[7:6]	Reserved	2	Do Not Use
5	OVP on DP_R PIN	1	0: OVP event has not occurred 1: OVP event has occurred
4	OVP on DN_L PIN	1	0: OVP event has not occurred 1: OVP event has occurred
3	OVP on SBU1 PIN	1	0: OVP event has not occurred 1: OVP event has occurred
2	OVP on SBU2 PIN	1	0: OVP event has not occurred 1: OVP event has occurred
1	OVP on GSBU1 PIN	1	0: OVP event has not occurred 1: OVP event has occurred
0	OVP on GSBU2 PIN	1	0: OVP event has not occurred 1: OVP event has occurred

SWITCHING SETTING ENABLE
Address: 04H
Reset Value: 8'b 1001_1000
Type: Read/Write

Bits	Name	Size	Description
7	Device Enable	1	0: Device Disable; L, R pull down by 10 k and other switch nodes will be high-Z for positive input. 1: Device Enable. Device Enable = 1 Device enable = 0 ENN=1 Device Disable Device Disable ENN=0 Device Enable Device Disable
6	SBU1_H to SBUx switches	1	0: Switch Disable; SBU1_H will be high-Z for positive input 1: Switch Enable
5	SBU2_H to SBUx switches	1	0: Switch Disable; SBU2_H will be high-Z for positive input 1: Switch Enable
4	DN or L to DN_L switches	1	0: Switch Disable; DN_L,DN will be high-Z for positive input. L pull down by 10 kohm 1: Switch Enable
3	DP or R to DP_R switches	1	0: Switch Disable; DP_R, DP will be high-Z for positive input. R pull down by 10 kohm 1: Switch Enable
2	Sense to GSBUx switches	1	0: Switch Disable; Sense,GSBU1 and GSBU2 will be high-Z for positive input 1: Switch Enable
1	MIC to SBUx switches	1	0: Switch Disable: MIC will be high-Z for positive input. 1: Switch Enable
0	AGND to SBUx switches	1	0: Switch Disable: AGND will be high-Z for positive input. 1: Switch Enable

SWITCH SELECT
Address: 05H
Reset Value: 8'b 0001_1000
Type: Read/Write

Bits	Name	Size	Description
7	Reserved	1	Do Not Use
6	SBU1_H to SBUx switches	1	0: SBU1_H to SBU1 switch ON 1: SBU1_H to SBU2 switch ON
5	SBU2_H to SBUx switches	1	0: SBU2_H to SBU2 switch ON 1: SBU2_H to SBU1 switch ON
4	DN or L to DN_L switches	1	0: DN_L to L switch ON 1: DN_L to DN switch ON
3	DP or R to DP_R switches	1	0: DP_R to R switch ON 1: DP_R to DP switch ON
2	Sense to GSBUx switches	1	0: Sense to GSBU1 switch ON 1: Sense to GSBU2 switch ON
1	MIC to SBUx switches	1	0: MIC to SBU2 switch ON 1: MIC to SBU1 switch ON
0	AGND to SBUx switches	1	0: AGND to SBU1 switch ON 1: AGND to SBU2 switch ON

SWITCH STATUS0
Address: 06H
Reset Value: 8'b 0000_0101
Type: Read

Bits	Name	Size	Description
[7:6]	Reserved	2	Do not use
[5:4]	Sense Switch Status	2	00: Sense switch is Open/Not Connected 01: Sense connected to GSBU1 10: Sense connected to GSBU2 11: Not Valid
[3:2]	DP_R Switch Status	2	00: DP_R Switch Open/Not Connected 01: DP_R connected to DP 10: DP_R connected to R 11: Not Valid
[1:0]	DN_L switch Status	2	00: DN_L Switch Open/Not Connected 01: DN_L connected to DN 10: DN_L connected to L 11: Not Valid

SWITCH STATUS1
Address: 07H
Reset Value: 8'b 0000_0000
Type: Read

Bits	Name	Size	Description
[7:6]	Reserved	2	Do not use
[5:3]	SBU2 Switch Status	3	000: SBU2 switch is Open/Not Connected 001: SBU2 connected to MIC 010: SBU2 connected to AGND 011: SBU2 connected to SBU1_H 100: SBU2 connected to SBU2_H 101: SBU2 connected both SBU1_H and SBU2_H 110…111: Do not use
[2:0]	SBU1 Switch Status	3	000: SBU1 switch is Open/Not Connected 001: SBU1 connected to MIC 010: SBU1 connected to AGND 011: SBU1 connected to SBU1_H 100: SBU1 connected to SBU2_H 101: SBU1 connected both SBU1_H and SBU2_H 110…111: Do not use

AUDIO SWITCH LEFT CHANNEL SLOW TURN-ON
Address: 08H
Reset Value: 8'b 0000_0001
Type: Read/Write

Bits	Name	Size	Description
[7:0]	Switch turn on rising time setting	8	11111111: 41840μs … 00000001: 344μs 00000000: 180μs

AUDIO SWITCH RIGHT CHANNEL SLOW TURN-ON
Address: 09H
Reset Value: 8'b 0000_0001
Type: Read/Write

Bits	Name	Size	Description
[7:0]	Switch turn on rising time setting	8	11111111: 41840μs … 00000001: 344μs 00000000: 180μs

MIC SWITCH SLOW TURN-ON
Address: 0AH
Reset Value: 8'b 0000_0001
Type: Read/Write

Bits	Name	Size	Description
[7:0]	Switch turn on rising time setting	8	11111111: 58870μs … 00000010: 680μs 00000001: 450μs 00000000: Not Valid

SENSE SWITCH SLOW TURN-ON
Address: 0BH
Reset Value: 8'b 0000_0001
Type: Read/Write

Bits	Name	Size	Description
[7:0]	Switch turn on rising time setting	8	11111111: 43550μs
			…
			00000001: 370μs
			00000000: 200μs

AUDIO GROUND SWITCH SLOW TURN-ON
Address: 0CH
Reset Value: 8'b 0000_0001
Type: Read/Write

Bits	Name	Size	Description
[7:0]	Switch turn on rising time setting	8	11111111: 425000μs
			…
			00000001: 3360μs
			00000000: 1700μs

TIMING DELAY BETWEEN R SWITCH ENABLE AND L SWITCH ENABLE
Address: 0DH
Reset Value: 8'b 0000_0000
Type: Read/Write

Bits	Name	Size	Description
[7:0]	Switch turn on rising time setting	8	11111111: 25500μs
			00000010: 200μs
			00000001: 100μs
			00000000: 0

TIMING DELAY BETWEEN MIC SWITCH ENABLE AND L SWITCH ENABLE
Address: 0EH
Reset Value: 8'b 0000_0000
Type: Read/Write

Bits	Name	Size	Description
[7:0]	Switch turn on rising time setting	8	11111111: 25700μs
			…
			00000010: 400μs
			00000001: 300μs
			00000000: 200μs

TIMING DELAY BETWEEN SENSE SWITCH ENABLE AND L SWITCH ENABLE
Address: 0FH
Reset Value: 8'b 0000_0000
Type: Read/Write

Bits	Name	Size	Description
[7:0]	Switch turn on rising time setting	8	11111111: 25550μs
			…
			00000010: 250μs
			00000001: 150μs
			00000000: 50μs

TIMING DELAY BETWEEN AUDIO GROUND SWITCH ENABLE AND L SWITCH ENABLE
Address: 10H
Reset Value: 8'b 0000_0000
Type: Read/Write

Bits	Name	Size	Description
[7:0]	Switch turn on rising time setting	8	11111111: 28500μs
			…
			00000010: 3200μs
			00000001: 3100μs
			00000000: 3000μs

AUDIO ACCESSORY STATUS
Address: 11H
Reset Value: 8'b 0000_0010
Type: Read

Bits	Name	Size	Description
[7:2]	Reserved	6	Do not use
1	CC_IN	1	0: CC_IN < 1.2 V 1: CC_IN > 1.5 V
0	DET	1	0: DET output is low 1: DET is output is high

FUNCTION ENABLE
Address: 12H
Reset Value: 8'b 0000_1000
Type: Read/Write

Bits	Name	Size	Description
7	Reserved	1	Do not use
6	DET I/O Control	1	1: DET pin is in Open/Drain Configuration 0: DET pin is in Push/Pull Configuration
5	RES detection range setting	1	1: 10k to 2560 k 0: 1k to 256 k
4	GPIO control enable	1	1: enable 0: disable
3	Slow turn on control enable	1	1: enable 0: disable
2	MIC auto break out control enable	1	1: enable 0: disable
1	RES detection enable	1	1: enable; will be changed to '0' after low resistance detection 0: disable
0	Audio jack detection and configuration enable	1	1: enable; will be changed to '0' after audio jack detection and configuration 0: disable

When GPIO control mode (manual switch control) is enable. 'Switch control' register is changed to read only. It will reflect switch status. I2C slave address is 0x42;

RES DETECTION PIN SETTING
Address: 13H
Reset Value: 8'b 0000_0000
Type: Read/Write

Bits	Name	Size	Description
[7:3]	Reserved	5	Do not use
[2:0]	Pin selection	3	000: CC_IN 001: DP/R 010: DN_L 011: SBU1 100: SBU2 101: Do not use … 111: Do not use

If RES detection pin is enable before setting PIN selection it will always do the CC_IN first. Recommend user to select the pin first before setting the RES detection pin enable.

RES VALUE
Address: 14H
Reset Value: 8'b 1111_1111
Type: Read

Bits	Name	Size	Description
[7:0]	Detected resistance value	8	0000_0000 : R < 1 k … 1111_1111: R > 300 K

RES DETECTION THRESHOLD
Address: 15H
Reset Value: 8'b 0001_0110
Type: Read/Write

Bits	Name	Size	Description
[7:0]	RES detection threshold	8	Selection by 1 K per step if Reg 12H[5] = 0 Selection by 10 K per step if Reg 12H[5] = 1 Default Value = 22 K /220 KΩ 0000_0000: 1 K /10 KΩ … 1111_1111: 256 K / 2560 K

RES DETECTION INTERVAL
Address: 16H
Reset Value: 8'b 0000_0000
Type: Read/Write

Bits	Name	Size	Description
[7:2]	Reserved	6	Do not use
[1:0]	RES detection interval	2	00: Single 01: 100 ms 10: 1 s 11: 10 s

AUDIO JACK STATUS
Address: 17H
Reset Value: 8'b 0000_0001
Type: Read

Bits	Name	Size	Description
[7:4]	Reserved	4	Do not use
3	4pole	1	1: 4 Pole SBU2 to MIC, SBU1 to audio ground 0: others
2	4pole	1	1: 4 Pole SBU1 to MIC, SBU2 to audio ground 0: others
1	3 pole	1	1: 3 pole 0: others
0	No audio accessory	1	1: No audio accessory 0: Audio accessory attached

RES DETECTION /AUDIO JACK DETECTION INTERRUPT FLAG
Address: 18H
Reset Value: 8'b 0000_0000
Type: Read Clear

Bits	Name	Size	Description
[7:3]	Reserved	5	Do Not Use
2	Audio jack detection and configuration	1	0: Audio jack detection and configuration has not occurred 1: Audio jack detection and configuration has occurred
1	Low resistance occurred	1	0: Low resistance has not occurred 1: Low resistance has occurred
0	Low resistance detection	1	0: Low resistance has not occurred 1: Low resistance has occurred

RES /AUDIO JACK DETECTION INTERRUPT MASK
Address: 19H
Reset Value: 8'b 0000_0000
Type: Read/Write

Bits	Name	Size	Description
[7:3]	Reserved	5	Do Not Use
2	Audio jack detection and configuration	1	1: Mask Audio jack detection and configuration has occurred interrupt
1	Low resistance occurred	1	1: Low resistance has occurred interrupt
0	Low resistance detection	1	1: Low resistance detection has occurred interrupt

AUDIO JACK DETECTION REG1 VALUE
Address: 1AH
Reset Value: 8'b 1111_1111
Type: Read

Bits	Name	Size	Description
[7:0]	Audio jack detection value	8	Resistance between SBU1 to SBU2

AUDIO JACK DETECTION REG2 VALUE
Address: 1BH
Reset Value: 8'b 1111_1111
Type: Read

Bits	Name	Size	Description
[7:0]	Audio jack detection value	8	Resistance between SBU2 to SBU1

MIC DETECTION THRESHOLD DATA0
Address: 1CH
Reset Value: 8'b 0010_0000
Type: Read/Write

Bits	Name	Size	Description
[7:0]	MIC detection threshold DATA0	8	MIC detection threshold DATA0 0010_0000: 300 mV

MIC DETECTION THRESHOLD DATA1
Address: 1DH
Reset Value: 8'b 1111_1111
Type: Read/Write

Bits	Name	Size	Description
[7:0]	MIC detection threshold DATA1	8	MIC detection threshold DATA1 1111_1111: 2.4 V

I2C RESET
Address: 1EH
Reset Value: 8'b 0000_0000
Type: W/C

Bits	Name	Size	Description
[7:1]	Reserved	7	Reserved
0	I2C reset	1	0: default 1: I2C reset

CURRENT SOURCE SETTING
Address: 1FH
Reset Value: 8'b 0000_0111
Type: Read/Write

Bits	Name	Size	Description
[7:4]	Reserved	4	Reserved
[3:0]	Current Source Setting	4	1111: 1500μA 0111: 700μA 0001: 100μA 0000: invalid

■ Functional Description

Over-Voltage Protection:

OCP96011 features over-voltage protection (OVP) on receptacle side pins that switches off the internal signal routing path if the input voltage exceeds the OVP threshold. If OVP is occurred, interrupt signal can be send by INT signal and FLAG data will provide information that which pin had OVP event.

Headset Detection:

OCP96011 integrates headset unplug detection function by detecting the CC_IN voltage. The function is always active when device is enabling. DET will be high when CC_IN is low (CC_IN < 1.2 V). When CC_IN = High (CC_IN > 1.5 V), DET will be released to low.

	Device Disable	Device Enable
CC_IN < V_{TH_L} = 1.2 V	DET = 0	DET = 1
CC_IN > V_{TH_H} = 1.5 V	DET = 0	DET = 0

MIC Switch Auto-off Function:

The function is active during control bit 0x12H bit[2] = 1. When CC_IN is high (CC_IN > 1.5 V) and L,R, Audio ground switches are under on status, MIC switch will be off and receptacle side pin will be connected to ground for 50μs first. Then it shows high-Z status under MIC switch is set on status.

Audio Ground Detection and Configuration:

The function is active when control bit 0x12H bit[0] = 1 and R, L, AGND switches are set to be on status. For type-C interface analog headset, the audio ground could be SBU1 pin or SBU2 pin. The function will provide autonomous detection and configuration to route MIC and audio ground signal accordingly.

During detection and configuration, the R, L, Sense, MIC and Audio ground switch will be off. After detection and configuration, R and L switches will turn on according to switch configuration and timing setting. MIC, Sense and Audio ground will turn on according to detection results and timing control setting.

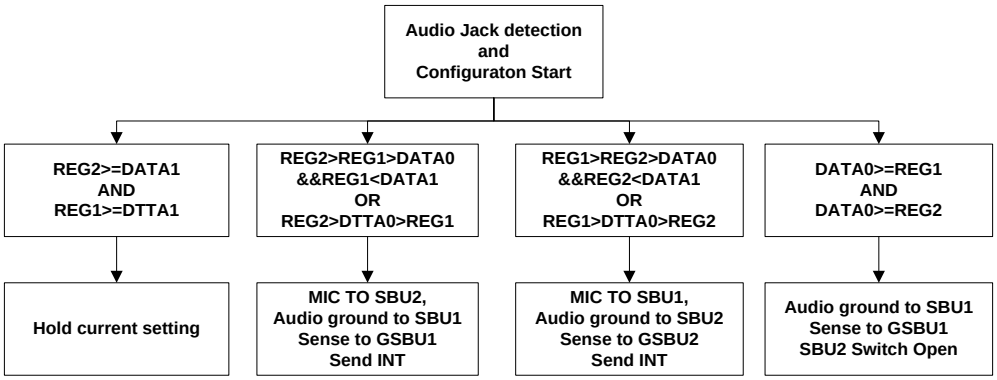


Figure4

Resistance Detection:

The function is active during control bit 0x12H bit [1] = 1. It will monitor the resistance between receptacle side pins and ground. During resistance detection, the switch which is monitored will be off. The detection result will be saved in the resistance flag register. The measurement could be from 1 k to 2.56 M which is controlled by internal register. The detection interval can be set at 100ms, 1 s or 10 s by register 0x16h.s

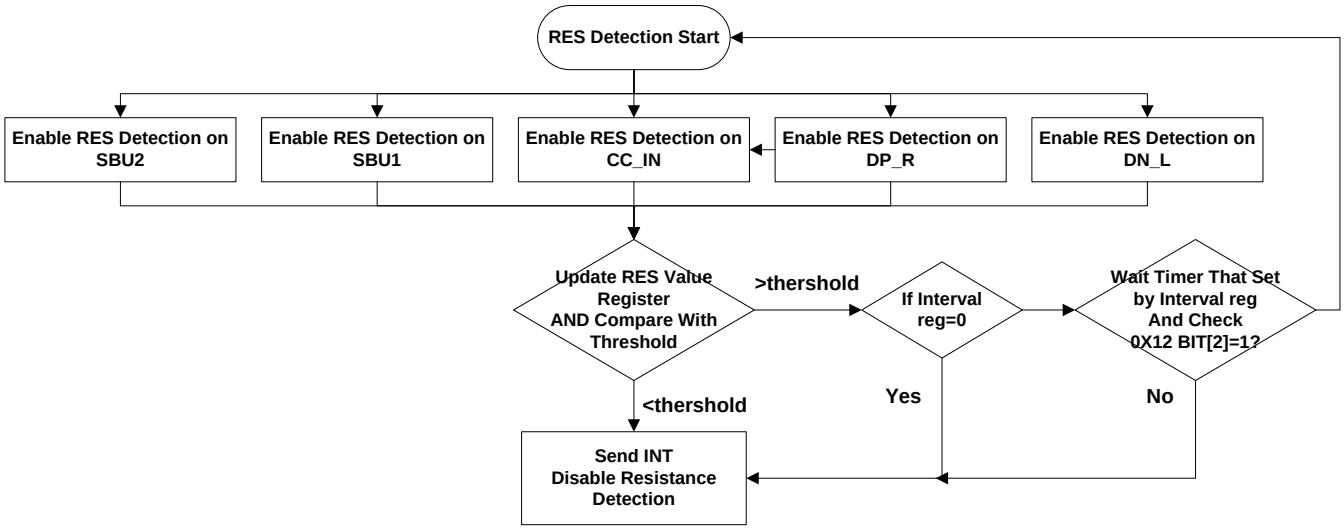


Figure5

MANUAL SWITCH CONTROL

(The function is active during control bit 0x12H bit [4] = 1 and 0x04H = FF. It will provide manual control for device. During this configuration, ADDR and INT pins will be set as logic control input.)

Power	ENN	ADDR	INT	SENSE Switch	Headset Detection	USB Switch	Audio Switch	MIC/ Audio GND Switch	SBU by Pass Switch
OFF	X	X	X	OFF	OFF	OFF	OFF	OFF	OFF
ON	H	X	X	OFF	OFF	OFF	OFF	OFF	OFF
ON	L	0	0	OFF	OFF	ON: DP_R to DP DN_L to DN	OFF	OFF	ON: SBU1 to SBU1_H SBU2 to SBU2_H
ON	L	0	1	OFF	OFF	ON: DP_R to DP DN_L to DN	OFF	OFF	ON: SBU1 to SBU2_H SBU2 to SBU1_H
ON	L	1	0	ON GSBU2 to SESNE	ON	OFF	ON: DP_R to R DN_L to L	ON: SBU1 to MIC SBU2 to Audio GND	OFF
ON	L	1	1	ON GSBU1 to SESNE	ON	OFF	ON: DP_R to R DN_L to L	ON: SBU2 to MIC SBU1 to Audio GND	OFF

OCP96011
TEST DIAGRAMS

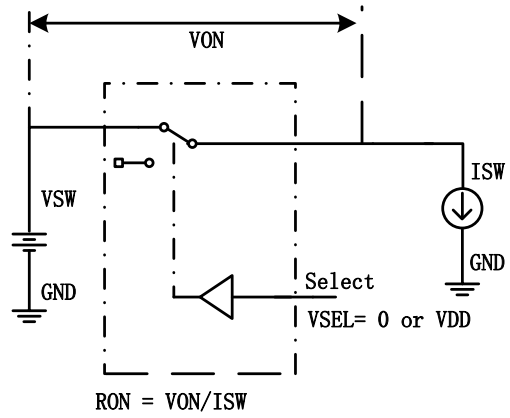


Figure6. On Resistance

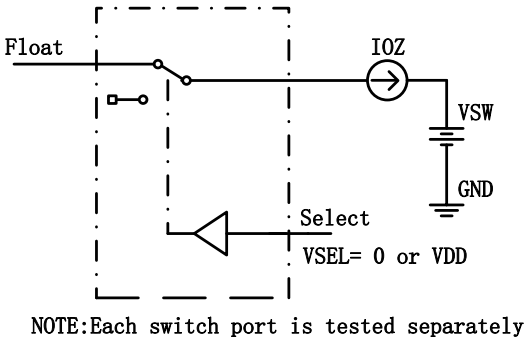


Figure7. Off Leakage (Ioz)

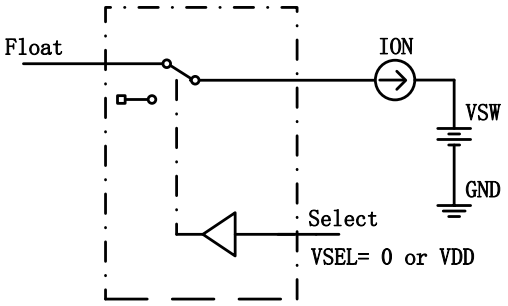


Figure8. On Leakage(Ion)

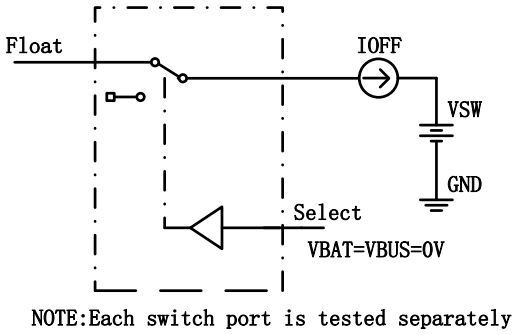


Figure9. Off Leakage (Ioff)

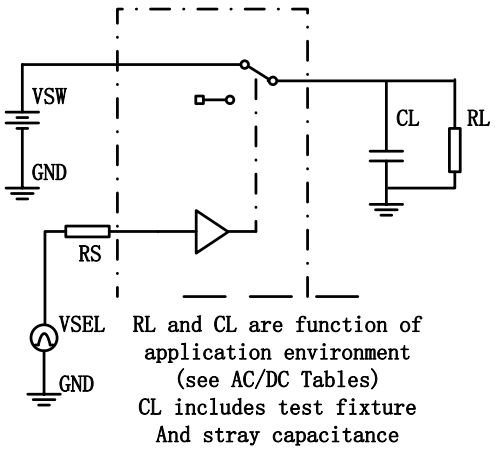


Figure10. Test Circuit Load

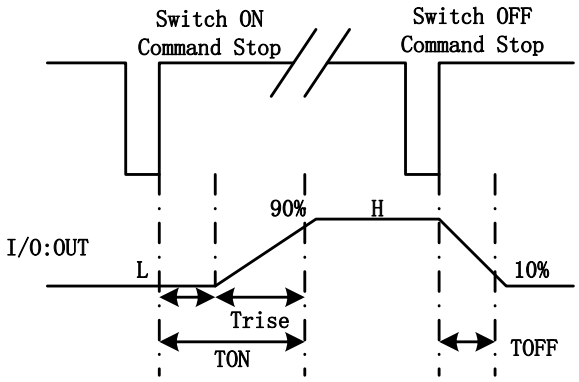


Figure11. Turn on/off Waveforms under Manual Mode

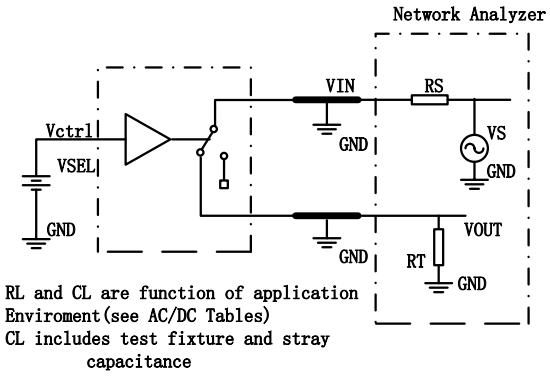


Figure12. Bandwidth

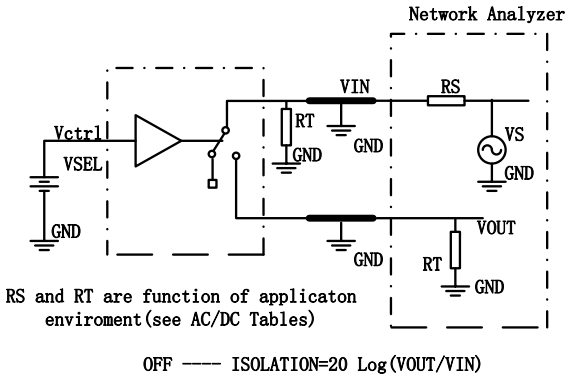


Figure13. Channel Off Isolation

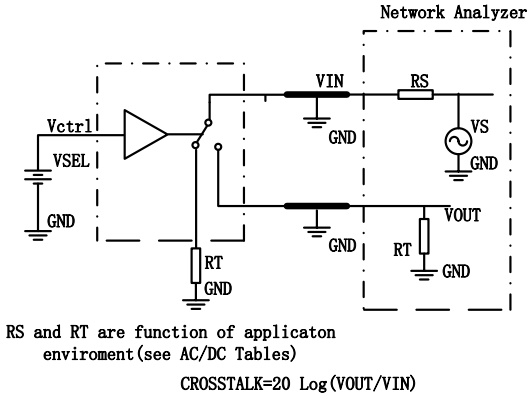


Figure14. Adjacent Channel Crosstalk

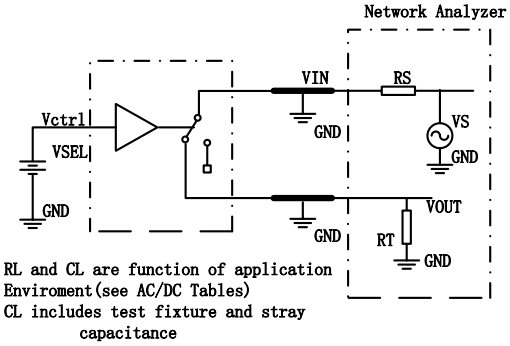


Figure15. Total Harmonic Distortion (THD+N)

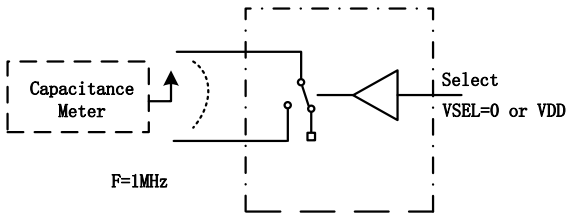


Figure16. Channel Off Capacitance

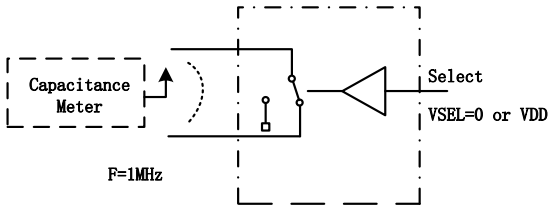


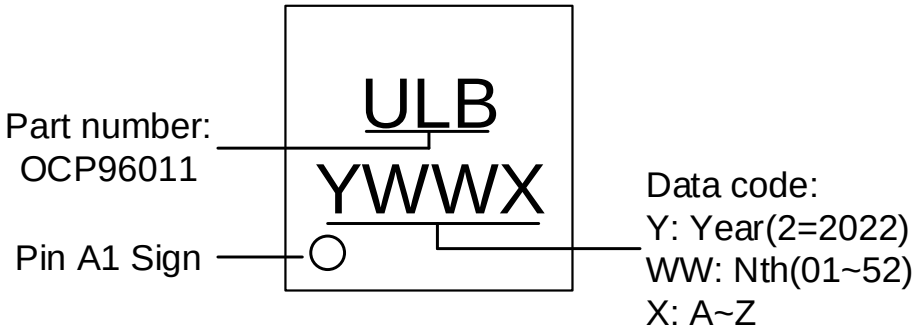
Figure17. Channel On Capacitance

■ Ordering Information

Part Number	Package Type	Package Qty	Temperature	Eco Plan	Lead/Ball Finish
OCP96011WPAD	25-Ball WLCSP	3000pcs	-40～85℃	Green	Sn/Ag/Cu

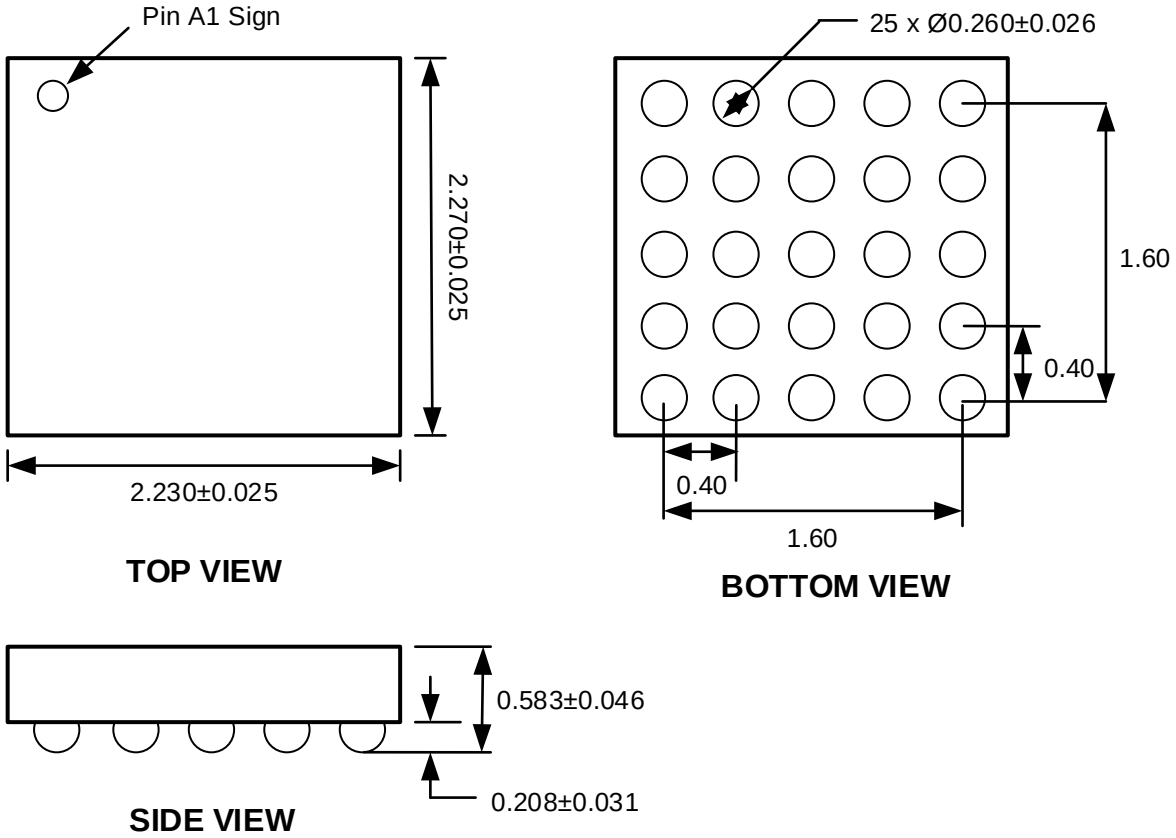
■ Marking Information

25-Ball WLCSP



■ Package Information

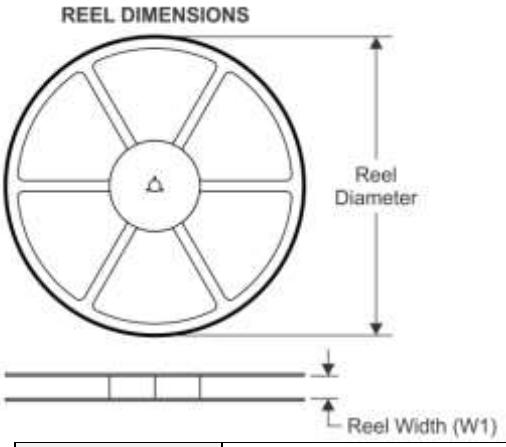
25-Ball WLCSP

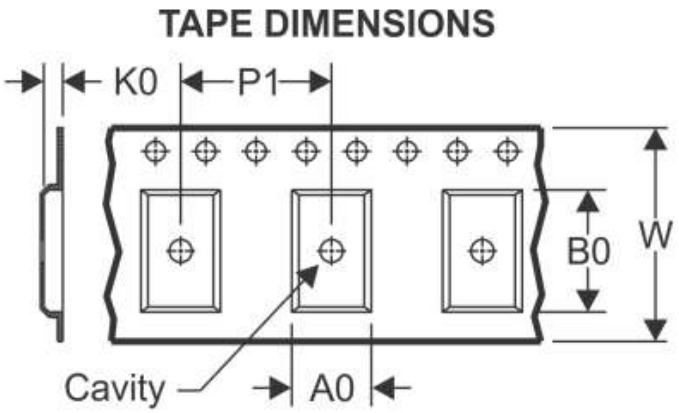


NOTE： ALL dimensions are in millimeters

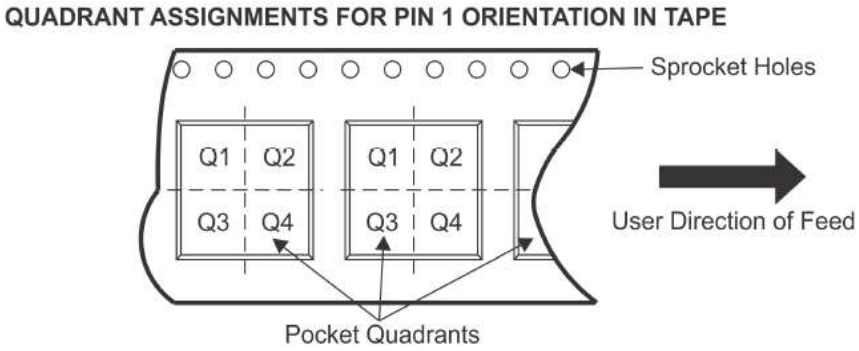
■ Packing Information

25-Ball WLCSP





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Package tape	Package Drawing	MSL	SPQ	Reel Diameter (mm)	Reel Width W1(mm)
25-Ball WLCSP (WLCSP-25B)	ULB	Level-1-260C	3000PCS	180	8.4
A0 (mm)	**B0 (mm)**	**K0 (mm)**	**P1 (mm)**	**W (mm)**	**PIN A1 Quadrant**
2.44	2.44	0.77	4.0	8.0	Q1

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